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## Stratix II DSP Performance

### Introduction

Stratix® II devices offer several digital signal processing (DSP) features that provide exceptional performance for DSP applications. These features include DSP blocks, TriMatrix™ memory, and three-input adder support; and make Stratix II devices ideal for the entire data path or as FPGA coprocessors for wireless infrastructure, broadcast television, medical imaging, and other signal and image processing applications.

This white paper discusses performance of Stratix II devices by examining the device architecture, Quartus® II software support, and DSP MegaCore® intellectual property (IP) support. Several examples show the benefits of Stratix II devices using readily available DSP IP from Altera.

### *Stratix II Device Architecture*

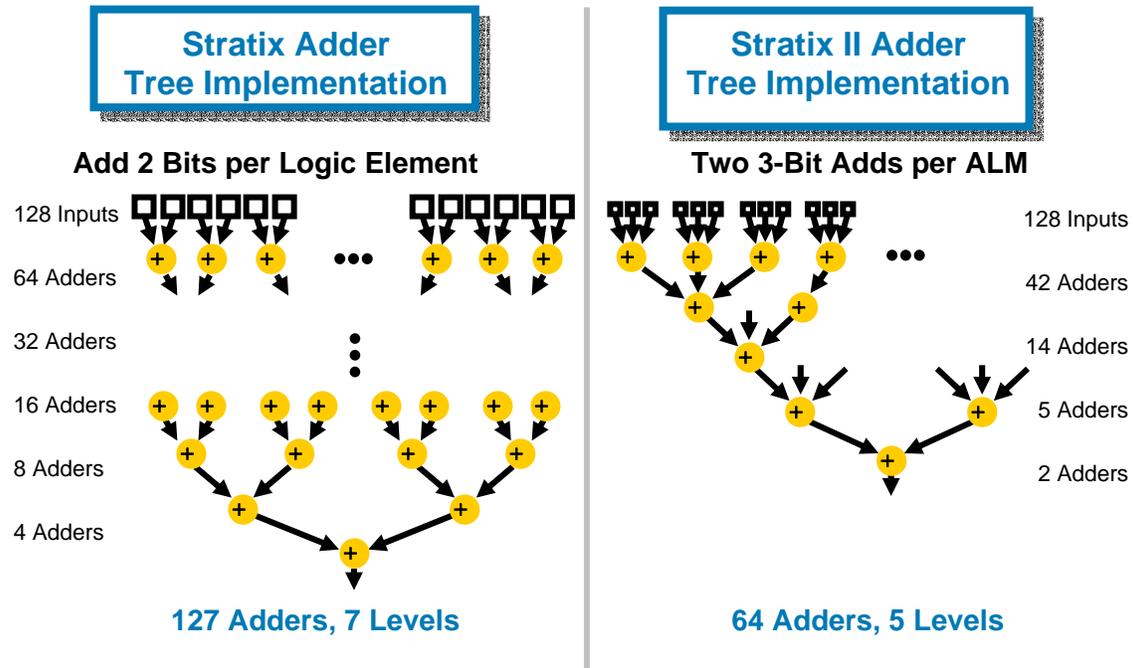
Stratix II DSP blocks deliver up to 420-MHz performance on 18-bit × 18-bit fully pipelined multipliers and can be configured to support the following modes:

- Up to eight 9-bit × 9-bit multipliers
- Up to four 18-bit × 18-bit multipliers
- Up to one 36-bit × 36-bit multiplier

Stratix II devices contain up to 96 DSP blocks or 384 18-bit × 18-bit multipliers, more than four times the number of DSP blocks found in Stratix devices. The Stratix II adaptive logic modules (ALMs) in the logic structure can be configured to efficiently support three-input adders so that two bits of three numbers can be added together in one ALM.

Figure 1 shows the benefits of Stratix II devices in designs such as filtering, which require large adder trees. The three-input adders lead to a reduction in the adder count of nearly 50%, which directly translates into logic resource savings.

Figure 1. Stratix II &amp; Stratix Comparison in Adder Tree Designs



The DSP blocks also have hardware support to perform optional saturation and rounding after each  $18 \times 18$  multiplier for Q1.15 input formats. This feature enables critical logic savings for algorithms such as speech compression. For more information on device architecture features, refer to the DSP Block section of *Stratix II Device Handbook, Volume 2*.

### Quartus II Software Support

The Quartus II software, version 4.2, has been optimized to support Stratix II device features, such as DSP Blocks and three-input adders. There are two distinct methods for implementing various modes of the DSP block in a design: instantiation and inference. Both methods use the following three Quartus II megafunctions:

- `lpm_mult`
- `altmult_add`
- `altmult_accum`

It is possible to instantiate the megafunctions in the Quartus II software to use the DSP block. Alternatively, with inference, it is possible to create an HDL design and synthesize it using a third-party synthesis tool such as LeonardoSpectrum, Synplify, or Quartus II Native Synthesis, which infers the appropriate megafunction by recognizing multipliers, multiplier adders, and multiplier accumulators. Using either method, the Quartus II software maps the functionality to the DSP blocks during compilation.

Refer to the Quartus II software online help for instructions on using the megafunctions and the MegaWizard® Plug-In Manager. For more information about synthesis tool inference support, refer to application note *AN 193: Design Guidelines for Using DSP Blocks in the Synplify Software* and *AN 194: Design Guidelines for Using DSP Blocks in the LeonardoSpectrum Software*.

Both the Parallel Adder megafunction (`parallel_add`) and synthesis inference are available for implementing the three-input adder. For example, the code `d = a + b + c` automatically maps to the three-input adder structure.

### DSP Megacore IP Support

Altera and its partners in the Altera Megafunction Partners Program (AMPP<sup>SM</sup>) offer a large selection of off-the-shelf megafunctions optimized for Altera devices. Designers can implement these parameterized blocks of IP easily, reducing design and test time. Altera has optimized the following DSP megacores for Stratix II device features such as DSP Blocks, TriMatrix Memory, and three-input adders:

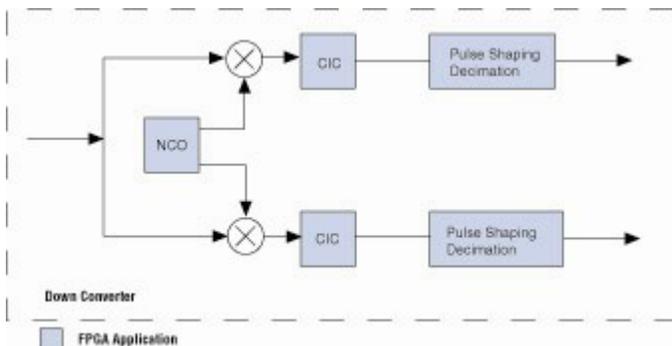
- Finite Impulse Response (FIR) Compiler
- Fast Fourier Transform (FFT) Compiler
- Numerically Controlled Oscillator (NCO) Compiler
- Viterbi Compiler
- Turbo Encoder/Decoder
- Reed Solomon Encoder/Decoder

### Examples using Altera's DSP Megacore IP

The following sections present examples that take advantage of the Stratix II device architecture and optimized DSP Megacore IP. The examples are based on FIR, NCO, and FFT, three very common DSP functions: The first example is a digital down converter for 3G wireless systems.

A digital down converter, shown in Figure 2, is used in wireless systems for translating signals from an intermediate frequency (IF) to a baseband frequency. A digital down converter typically consists of an NCO, an FIR filter (pulse shaping decimation filter), a mixer, and an optional cascaded integrator comb (CIC) filter.

Figure 2. Block Diagram for a Generic Digital Down Converter



## NCO

Because of the 3G wireless systems' stringent requirements, NCOs must generate very high-quality signals as measured by spurious free dynamic range. A typical spurious free dynamic range requirement for 3G is for the magnitude to be greater than  $[-110 \text{ dB}]$ . This block can be implemented with Altera's NCO Compiler 2.2.0 using the following parameters, based on the *NCO MegaCore Function User Guide*:

- Phase accumulator precision 32 bits
- Angular precision 18-bits
- Magnitude precision 18-bits
- Multiplier based algorithm
- Dithering ON

Figure 3 shows a frequency response that meets the 3G wireless requirements for an NCO.

Figure 3. NCO Frequency Response

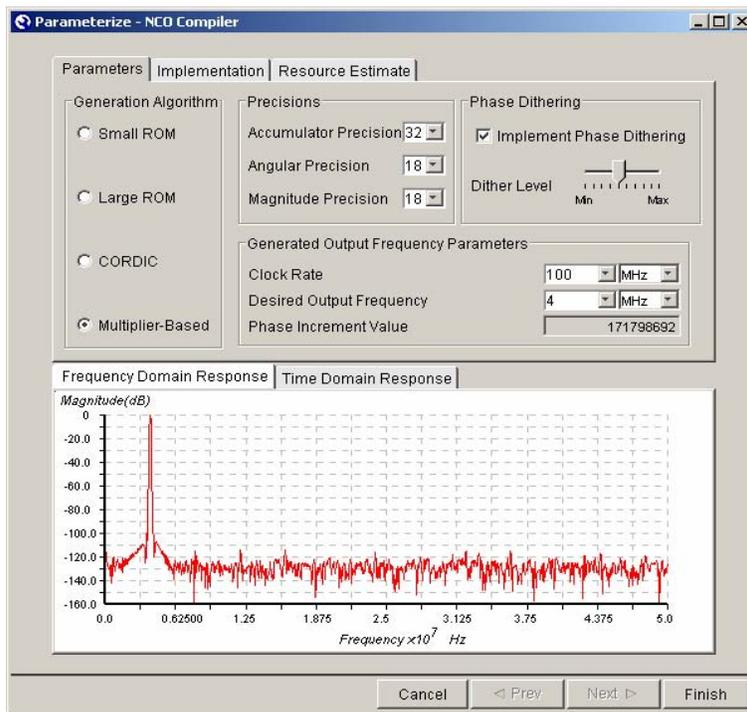


Figure 3 shows that the device meets the spurious free dynamic range requirements of greater than  $[-110 \text{ dB}]$ . This NCO design implemented in Stratix II devices gives a performance improvement of 25% over Stratix devices, because of the increased performance of the Stratix II DSP blocks, M4K memory, and the new logic structure.

Table 1 summarizes the resource utilization and performance of Stratix II devices.

Table 1. NCO Resource Utilization and Performance in Stratix II Devices

Parameter	Stratix II
LEs (1)	236
Memory usage (M4K)	6
DSP block 9-bit elements	8
Speed ( $f_{\max}$ )	361 MHz

**Notes to Table 1:**

(1): The LE count in Stratix II devices refers to the ALUTs reported in the Quartus II software.

## FIR

The decimating FIR filter for 3G applications requires over 65 dB of out-of-band signal rejection. A typical system clock rate is a multiple of the channel bandwidth of 3.84 MHz for 3G systems. Many systems use 61.44 MHz ( $3.84 \times 16$ ) as the system clock rate. The following example shows how to achieve those specifications using Altera's FIR Compiler 3.2. As an engineering experiment, the following parameters for a 3G decimating filter were chosen to meet the design requirements:

- 14-bit data
- 14-bit coefficients
- 120-tap Filter
- pipeline =1
- # of channels = 1
- multi-bit serial architecture

Figure 4 shows a typical frequency response curve for an FIR.

Figure 4. FIR Frequency Response

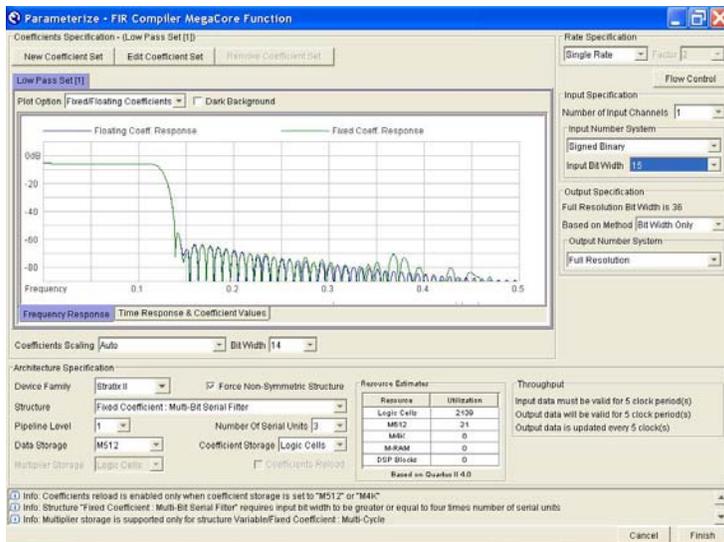


Table 2 compares the common parameters that characterize Stratix and Stratix II devices.

*Table 2. FIR Benchmark Comparison Between Stratix & Stratix II Devices*

Parameter	Stratix	Stratix II
Adder tree type	Binary	Ternary
Number of adders	123	73
LEs (1)	3,691	1,776
Memory usage (M512)	28	21
Speed (f <sub>max</sub> )	248 MHz	373 MHz

**Notes to Table 2:**

(1): The LE count in Stratix II devices refers to the ALUTs reported in the Quartus II software.

The FIR Compiler 3.2 provides a multi-bit serial architecture, which allows the users to optimize their designs to a specific performance requirement. Adding multiple serial engines achieves higher performance by adding parallelism. The number of serial engines required is defined by the following equation:

$$\# \text{ of Serial Units} = \text{Round} (\text{Data Bit Width} \times \text{Required Filter Performance} / \text{Filter Fmax})$$

$$\text{Stratix \# of Serial Units} = \text{Round} (15 \times 61.44 \text{ MHz} / 248 \text{ MHz}) = 4$$

$$\text{Stratix II \# of Serial Units} = \text{Round} (15 \times 61.44 \text{ MHz} / 373 \text{ MHz}) = 3$$

In this way, the 24% increase in f<sub>max</sub> performance permits a 20% smaller design. The ternary adder capability within Stratix II devices reduces the number of adders within each serial unit, leading to an additional reduction in the logic resource usage. A Stratix II architecture can implement this design with 50% less logic resources and 25% less memory resources than Stratix architectures. This design equates to 8.9 GMACs (over twice the speed of the fastest DSP processors available – 720 MHz × 4 16 × 16 MACs) and uses less than 1% of an EP2S180 device's logic resources (1,776 of 179,400 Logic Elements).

## FFT

An FFT is used in applications such as OFDM modems, filtering in the frequency domain, and spectrum analysis. Some of the most advanced spectrum analysis applications require a 1K-point FFT to be calculated in less than 2  $\mu$ s at 16-bits of precision. The FFT core generated by the FFT Compiler 2.1 targeting Stratix II devices can now achieve this using a dual engine, quad output, buffered burst architecture.

Figure 5 shows the multiplier and memory options that are available with the FFT.

Figure 5. FFT Implementation Options

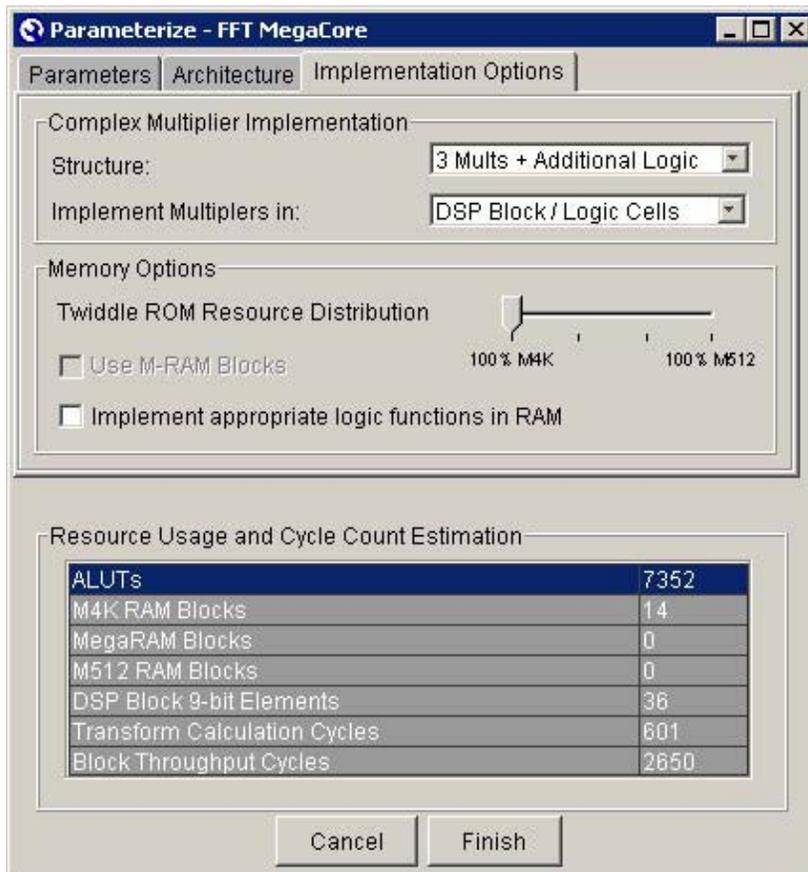


Table 3 summarizes the resource utilization and performance for Stratix II devices with this FFT design.

*Table 3. 1K-Point FFT Resource Utilization & Performance for Stratix II Devices*

Parameter	Stratix II
LEs (1)	6,660
Memory usage (M4K)	14
DSP block 9-bit elements	36
Speed ( $f_{max}$ )	300 MHz
Cycles (excl data load: 557 cycles)	—
Transform calculation time	1.9 s

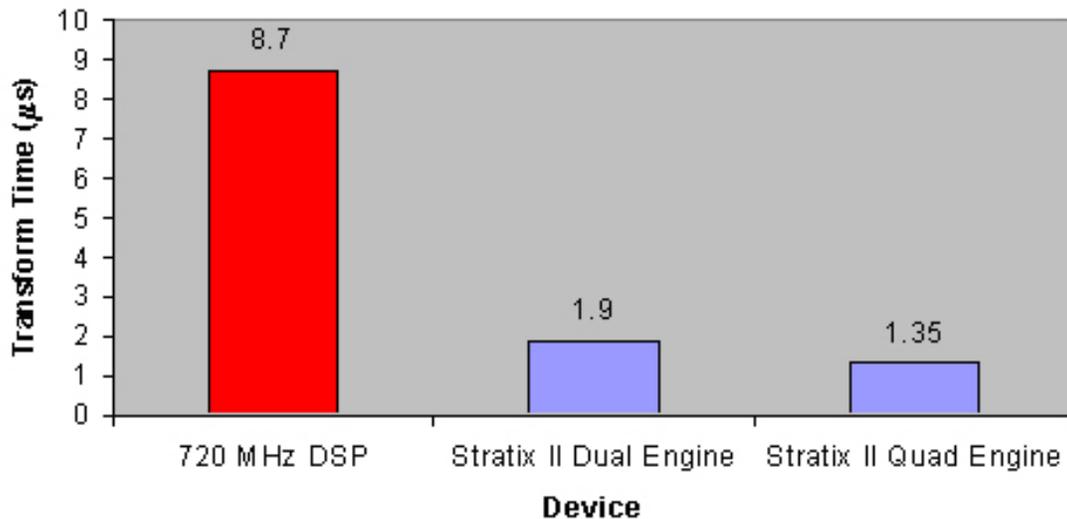
*Notes to Table 3:*

(1): The LE count in Stratix II devices refers to the ALUTs reported in the Quartus II software.

The Stratix II implementation provides a 21% performance improvement over Stratix devices when designing this FFT. Using Altera's Quad Engine, Quad Output Architecture, this same FFT can be implemented in Stratix II with a transform calculation time of only 1.35 s. Furthermore, when compared to a 720-MHz discrete DSP processor, the FFT core is seven times faster and can fit in the smallest Stratix II device, the EP2S15.

Figure 6 shows the contrast in speed among various devices

*Figure 6. 16-Bit Fixed-Point, 1,024-Point FFT Performance Comparison*



## Summary

Stratix II devices deliver DSP performance in the range of 300 to 400 MHz, providing significant speed increases in the DSP blocks and logic resources, as compared with Altera's Stratix family of devices. In many cases, such as in the FIR Filter example, this increase can lead to a significant reduction in logic resources for a given performance requirement, resulting directly in a lower cost design. Refer to the *Stratix II Device Performance & Logic Efficiency Analysis* white paper for detailed information on the performance of Stratix II devices and the increased efficiency that the new and innovative logic structure offers.



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