Gate Dielectric Scaling for High-Performance CMOS: from SiO2/PolySi to High-K/Metal-Gate

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Content

• Introduction
• SiO2 Scaling
• Review on High-K Problems
• Significant Breakthroughs in High-K/Metal-Gate
• High-K/Metal-gate NMOS & PMOS Transistors with Record-Setting Drive Performance
• Summary
Introduction

- 1.2nm physical SiO2 in production in our 90nm logic technology node
- 0.8nm physical SiO2 in our research transistors with 15nm physical Lg
- Gate leakage is increasing with reducing physical SiO2 thickness
- SiO2 running out of atoms for further scaling
- Will eventually need high-K
SiO2 Scaling

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors
Electrical Characteristics of 0.8nm Physical SiO2 & PolySi Gate

Inversion Capacitance

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Research Transistor with 15nm Physical Lg and 0.8nm Physical SiO2 and PolySi Gate

- Well-controlled short-channel characteristics

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Sequential introduction of precursor molecules $\text{MCl}_4(\text{g})$ and $\text{H}_2\text{O}(\text{g})$; $\text{M}=$\text{Zr} or $\text{M}=$\text{Hf}
Review on High-K Problems (High-K/PolySi-Gate)

• High-K and polySi gate are incompatible due to Fermi level pinning at the high-K and polySi interface which causes high threshold voltages in transistors

• High-K/polySi transistors exhibit severely degraded channel mobility due to the coupling of SO phonon modes in high-K to the inversion channel charge carriers
High-K and PolySi are Incompatible

• Defect formation at the polySi-high-K interface

• TCAD simulation shows it takes only 1 defect out of 100 surface atoms to “pin” the transistor threshold voltage (high Vth)

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Mobility Degradation in High-K/PolySi

Inversion Electron Mobility (cm$^2$/V.s) vs Electric Field (MV/cm)

- Universal Mobility
- SiO$_2$ / Poly-Si
- High-K / Poly-Si

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Problems of High-K/PolySi Transistors

PolySi/SiO2
Toxe = 20Å

PolySi/High-K
Toxe = 17Å

[Higher Vth and lower mobility]

Vd = 1.3V
Lg = 110nm
Experimental Evidence of Phonon Scattering in High-K/PolySi Gate

\[ \frac{d(1/\mu_{eff})}{dT} = \frac{1}{\mu_{Coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{SR}} \]

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Review on High-K Problems (High-K/Metal-Gate)

• Metal gate electrodes are able to screen the high-K SO phonons from coupling to the inversion channel charge carriers and reduce the mobility degradation problem

• However the use of high-K/metal-gate requires metal gate electrodes with the “correct” work functions on high-K for both PMOS and NMOS transistors for high performance
Significant Breakthroughs in High-K/Metal-Gate made by Intel

- N-type metal and P-type metal with the correct work functions on high-K have been engineered and demonstrated for high-performance CMOS
- High-K/metal-gate stack achieves NMOS and PMOS channel mobility close to SiO2’s
- High-K/metal-gate stack shows significantly lower gate leakage than SiO2
We have Engineered N-type and P-type Metal Electrodes on High-K with the “Correct” Work Functions for NMOS and PMOS on Bulk Si
High-K/n-type Metal-Gate Stack Achieves NMOS Channel Mobility Close to SiO2

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High-K/p-type Metal-Gate Stack Achieves PMOS Channel Mobility Close to SiO2

PMOS Mobility (cm²/V.s) vs. Inversion Electrical Thickness, Toxe (Å)

- SiO2/PolySi
- High-K/p+ Metal-Gate

E_{eff} = 1.0MV/cm
High-K Reduces Gate Leakage

Accumulation Electrical Tox [A]

Jox [A/cm^2]

SiO2/polySi

High-K/metal-gate

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High-K/Metal-gate NMOS and PMOS Transistors with Record-Setting Drive Current (Idsat) Performance

• NMOS and PMOS high-K/metal-gate transistors were made on bulk Si
  – Physical gate length (Lg) = 80nm
  – Electrical Oxide Thickness @ inversion (Toxe) = 1.45nm

• Record-setting NMOS Idsat
  – Idsat = 1.66mA/um, Ioff = 37nA/um at Vcc = 1.3V

• Record-setting PMOS Idsat
  – Idsat = 0.69mA/um, Ioff = 25nA/um at Vcc = 1.3V
High-K/Metal-Gate NMOS with Record-Setting Drive Current Performance

- Electrical Tox at Inversion (Toxe) = 1.45nm
- Transistor physical gate length (Lg) = 80nm

Ion = 1.66mA/um
Ioff = 37nA/um
Lg = 80nm
Toxe = 14.5A
High-K/Metal-Gate PMOS with Record-Setting Drive Current Performance

- Electrical Tox at Inversion (Toxe) = 1.45nm
- Transistor physical gate length (Lg) = 80nm
Summary

- We have implemented 1.2nm physical SiO2 in our 90nm logic technology node and products, and have demonstrated 0.8nm physical SiO2.
- We have engineered and demonstrated NMOS and PMOS high-K/metal-gate stacks on bulk Si with i) the correct work functions, ii) channel mobility close to SiO2’s and iii) very low gate leakage.
- We have fabricated high-K/metal-gate NMOS and PMOS transistors on bulk Si with record-setting drive current performance.
- We believe high-K/metal-gate is a key technology option for the 45nm logic technology technology node, to be in production in 2007.