



Enabling 5G Fronthaul

An overview of standards, technologies, and intellectual property (IP) solutions to move the communications industry forward

Key components of 5G technology

Massive multiple-input multiple-output (MIMO): Advanced MIMO antenna technology, including adaptive digital/analog beamforming, beam tracking, and null steering techniques, reduces interference between cells. As users can be isolated using their spatial diversity, massive MIMO offers big spectral efficiency gains. This increases the throughput, data rate, coverage, and capacity of basestations.

Millimeter wave: Current mobile networks typically use the 700 MHz to 2.5 GHz spectrum, which is getting crowded due to the explosion of data from smart phones and other connected devices. Typical 5G New Radio (NR) mobile networks are focused on sub-6 GHz (3.5–4.5 GHz) and the 28/60 GHz spectrum, known as millimeter wave or mmWave, available for the first time for mobile broadband communications. The associated leap in performance can deliver fiber-like speeds, without the wires.

Small cells: Millimeter waves do not propagate through objects well; their energy is absorbed by buildings, plants, and rain. 4G is primarily based on large basestations broadcasting signals over long distances—this will not scale for 5G. In order to scale, 5G will use thousands of low-power mini basestations.

Executive summary

Cellular networks have been evolving at a frenetic pace in an effort to meet increasing demands from businesses, consumers, and a digital, data-driven economy. 5G represents another paradigm shift—one that requires rearchitecting networks and rethinking data centers. Both networking standards and technologies are changing to meet the demand and create new opportunities. In fronthaul networks, the recent merger of xRAN and C-RAN Alliance to form the ORAN Alliance is helping communications solution providers move forward.

In addition to helping drive open standards, Intel® reference architectures such as FlexRAN, Intel® FPGAs, and Intel® Programmable Acceleration Cards (Intel® PACs) are some of the ways Intel is enabling architecture to handle massive data loads and prepare for 5G. Here you will find an overview of the landscape, technical and industry challenges, and innovative solutions for the next wave of cellular networking.

Disruptive shifts in cellular networks

Mobile cellular networks have evolved continuously and dramatically. We've seen the shift from 2G voice cellular communications to support data in the late 1990s; the app revolution in 3G in the early 2000s; and faster data rates with 4G entering 2010.

5G represents a new network of networks—bringing the worlds of wireless, computing, and cloud together. It's about connecting things as much as connecting people. 5G will connect nearly everything, including billions of people and tens of billions of things. Enterprises such as smart cities, factories, and hospitals, as well as consumers, will utilize and consume data and drive network slices and services. The common denominator in 5G is the explosion of data used in intelligent networks for analytics and behavior tracking, responsiveness, and analysis. This unprecedented scale and scope will require a completely rearchitected network. In essence, 5G networks are smart, reactive, and will power new digital services and experiences.

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5G challenges

As you can see, 5G is a fundamentally different technology in terms of how the physical layer of the technology works. We will explore the requirements and challenges of 5G and how they can be addressed by various network elements. Network hardware elements, such as user equipment, modems, and antennas, operating at the physical layer need to work at a much higher speed and support greater bandwidth.

Fast-forward to modern 4G deployments and a typical use case has fiber from the BBU to an RRU colocated with the antenna, with the line rate around 10 Gbps. Although this progression was rapid, the underlying concept remained consistent. For the most part, the only changes to this application and vendor-specific interface was a simple increase in line rate. In 5G, this is all poised to change, dramatically.

From a business perspective, operators have long desired an application-neutral, vendor-interoperable interface to enable flexibility and multivendor system interoperability, and to reduce technical and inventory dependencies. Therefore, the drive has been toward an open, interoperable Ethernet interface and protocol—opening a path to and congruent with network functions virtualization (NFV).

Many 5G, and some new 4G, use cases demand a significant increase in fronthaul bandwidth. To address the increased cost of high-bandwidth fronthaul, architects have suggested new functional partitions between the BBU and RRU. One way to reduce the fronthaul bandwidth is to move functions from the BBU into the RRU. Another is through data compression techniques.

The 3GPP standards body defines the majority of mobile communications elements, testing, and interoperability. However, they have not defined the fronthaul interface. Previously, this gap was filled by CPRI. For 5G- and Ethernet-based transport, several groups have stepped forward to fill the specification gap.

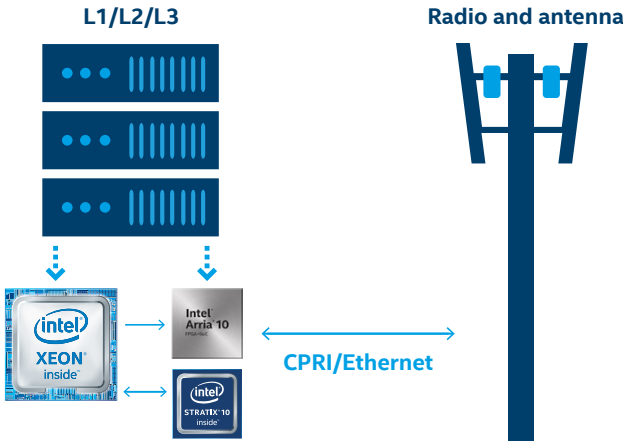


Figure 1. Baseband units (BBUs) and remote radio unit (RRU) with fronthaul interface

Impact of 5G on the fronthaul interface

5G data is delivered to users over the air using the radio frequency transmission and reception between radio basestations and terminals. In the 3GPP Radio Access Networks (RAN) definition, the radio basestation or digital unit (DU) is connected to the core network or central unit (CU) through a backhaul interface, while it is connected to the radio antennas or transmit-receive point (TRP) through the fronthaul interface.

For example, a remote radio unit (RRU) utilizing 3G was previously supporting two antennas covering 15 MHz of spectrum in traditional frequency bands <2.1 GHz. Now with 5G, this RRU/TRP needs to support up to 256 antennas, up to 200 MHz of spectrum <6 GHz, or up to 800 MHz in mmWave space >6 GHz in a similar mechanical footprint.

Looking back to the early days of fronthaul, in 2003 the first specification for a fronthaul interface was published by the Common Public Radio Interface (CPRI) consortium. CPRI was a closed forum driven by top wireless OEMs trying to define the transport mechanisms for digitized waveforms while maintaining all of the proprietary tricks to enable system-level differentiation. At that time, a common case employed copper cables to connect baseband units (BBUs) and colocated radio units at 614.4 Mbps.

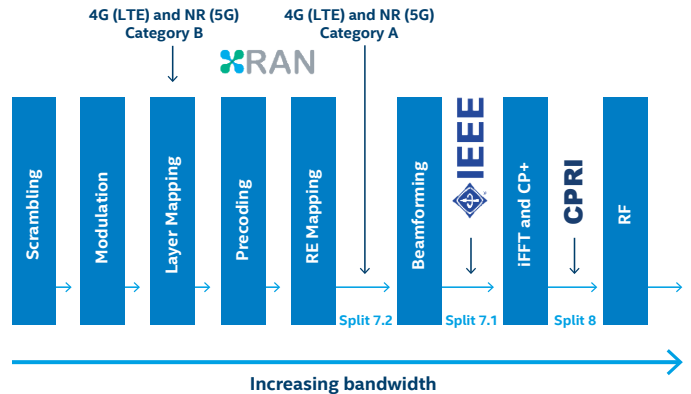


Figure 2. Layer 1 processing chain and 3GPP split points

Specification landscape

The 2015 IEEE1914.3-2018 Standard for Radio over Ethernet (RoE) Encapsulations and Mappings was the first action in defining a protocol for encapsulating fronthaul traffic in Ethernet frames. It allows backward compatibility by converting to/from Ethernet from/to CPRI. The standard specifies the transport protocol for both frequency domain and time domain data, at 3GPP functional split points 8 and 7.1.

The CPRI consortium published a new specification, eCPRI, in 2017. This is similar to the original CPRI specification in that much is left to be specified by each vendor. eCPRI does not define any specific functional split point (the original CPRI used split 8), but the transport mechanism is now Ethernet-based rather than application specific.

In 2016, Intel and others founded xRAN. At Mobile World Congress (MWC) Americas 2018, xRAN merged with the C-RAN Alliance, forming the ORAN Alliance. The xRAN/ORAN fronthaul specification defines a fronthaul interface and management plane over Ethernet or IP and specifies the transport protocol for frequency domain data at 3GPP functional split point 7.2. It can use either eCPRI or IEEE1914.3 for its common header.

Technical drivers

Typical 4G radios employ either two, four, or eight antennas. A new technology, massive MIMO typically has 64, 128, and 256 antennas. For the traditional CPRI interface, this would result in a 32x increase in fronthaul bandwidth. This increase in fronthaul bandwidth results in a massive and unviable increase in fronthaul cost. There is also a trade-off in complexity between engineering and costs. The more functions that are moved from the BBU to the RRU, the lower the cost of the fronthaul, but the consequence is an RRU higher in cost and complexity. Different vendors and use cases demand different functional splits for cost optimization. This is an ideal application to leverage the best combination between the Intel Xeon Scalable processor CPU and Intel® FPGA technology. This is also where Intel's compression IP becomes highly valuable to enable bandwidth-optimized links.

Moving from CPRI's dedicated, application-specific interface to Ethernet allows switching functions to be performed on white-box Ethernet switches. This provides advantages in terms of cost and competition, but also some technical challenges. The fronthaul interface is very time sensitive and demands very deterministic latency (CPRI requires better than +/- 10 ns accuracy). Ethernet was not designed to transport data with this level of time sensitivity or deterministic latency. The introduction of time synchronization mechanisms such as IEEE1588v2 and time-sensitive networking IEEE802.1CM standards allows for mitigating such requirements.

Solution: FlexRAN and Intel PACs

Wireless basestations, like most network nodes, have traditionally been vertically integrated boxes. FlexRAN is an end-to-end Intel reference architecture to implement software-based radio stations, which can sit on any part of the wireless network from edge to core. A FlexRAN platform solution performs the entire 4G and/or 5G layer 3, 2, and 1 processing. Intel Xeon Scalable processors are used to implement layers 3 and 2 and some of layer 1, and Intel FPGAs are used to perform acceleration of the remainder of layer 1 and the fronthaul connectivity.

Uniform software architecture supporting different deployment models

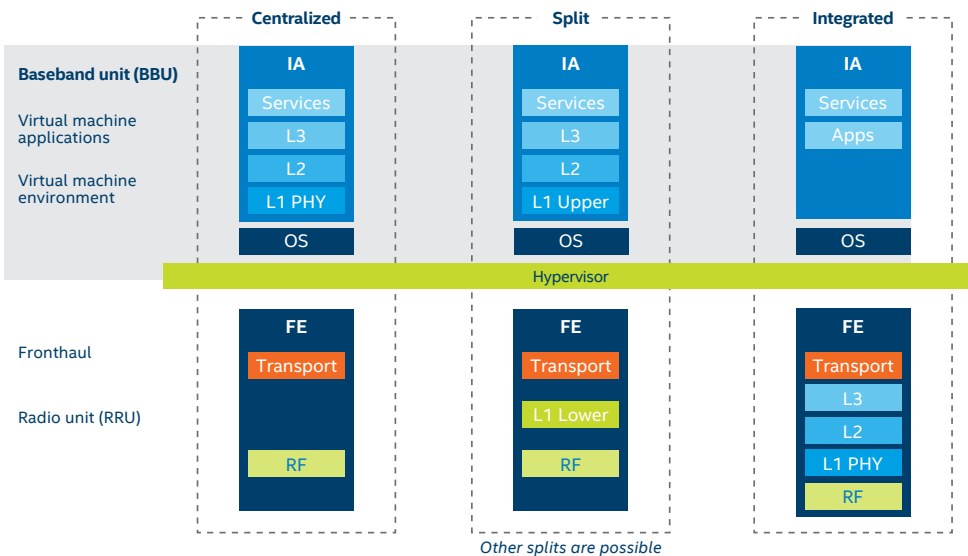


Figure 3. Intel® wireless access solution architectures

Partitioning the 5G protocol stack

The partitioning of the 5G protocol stack functions fluidly, unlike 4G, where it was more fixed. This means that basestations can now support centralized, integrated, and hybrid architecture splits to meet the requirements of specific use cases. Fronthaul protocols have been thoroughly revisited to support different partitioning schemes while maintaining the connectivity and timing requirements for each split.

Given the number of different standards and proprietary flavors of fronthaul protocols, Intel FPGAs offer the ideal

platform—providing the flexibility required to efficiently handle interface and bit manipulation functions. Intel enables a seamless integration of Intel FPGA acceleration within the FlexRAN hardware and software environment with Intel PACs tailored for 4G and 5G compute requirements.

Intel FPGAs and software IP are available for the traditional CPRI standard and for next-generation fronthaul interfaces such as IEEE1914.3 RoE and xRAN/ORAN.

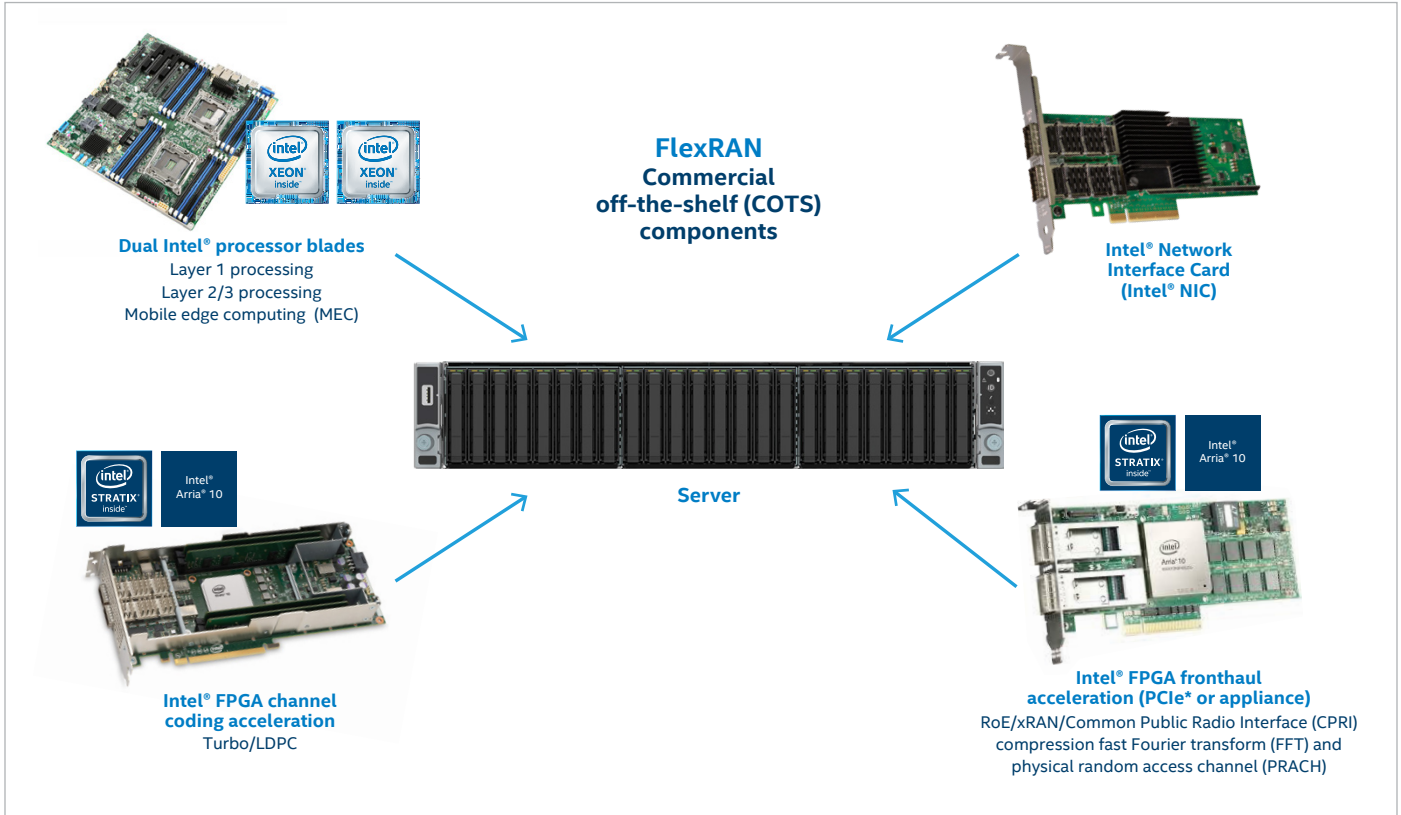
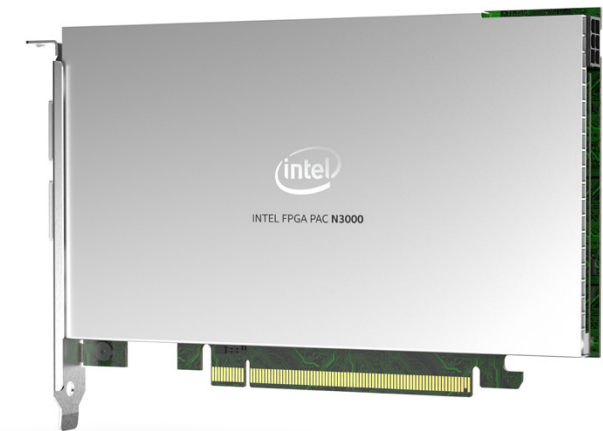


Figure 4. FlexRAN system architecture



Intel PACs

The Intel® Programmable Acceleration Card for Networking (Intel® PAC N3000) provides multiple solutions for data center and wireless applications. In the wireless infrastructure space, the Intel FPGA and Intel® NIC on the Intel PAC are used to implement both fronthaul acceleration and channel coding. As the card is programmable, it can be used to implement any fronthaul standard (CPRI, IEEE1914.3, eCPRI, and xRAN/ORAN) plus lower layer channel coding functions such as Turbo (4G) and/or LDPC/Polar (5G) channel coding. The Intel PAC also has a wealth of memory options for performing hybrid automatic repeat request (HARQ) processing.

Sample use case and migration path using Intel PAC

Figure 5 shows a sample use case and the migration path of a centralized vRAN from 4G to 5G.

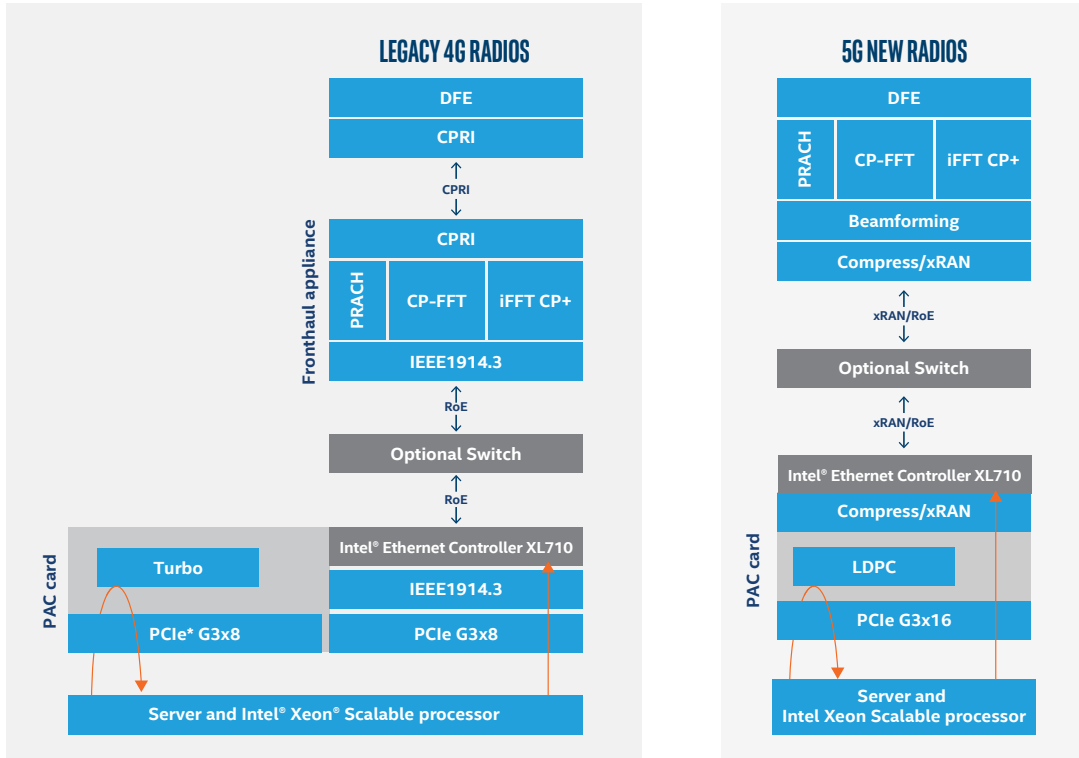


Figure 5. Migration from 4G to 5G with the Intel® PAC N3000

On the left, our 4G centralized vRAN PAC is ultimately connecting to existing legacy CPRI-based RRU. The Intel PAC plugs into the server and provides look-aside acceleration (6 Gbps DL and 3 Gbps UL) for Turbo and bump-in-the-wire acceleration and compression for an Ethernet-based fronthaul interface such as IEEE1914.3 RoE. A fronthaul appliance then performs the processing between split 7.1 and 8 to provide multiple CPRI connections to multiple RRUs.

On the right, the same Intel PAC hardware is used. However, it has now been reprogrammed to provide look-aside acceleration for LDPC/Polar and/or HARQ and bump-in-the-wire acceleration and compression for xRAN or RoE. A fronthaul appliance is no longer necessary because it is assumed that new 5G radios will perform the processing between split 7.x and 8, and that the RRU will be xRAN and/or RoE compatible.

At MWC Shanghai in 2018, Intel demonstrated the left-hand column for fronthaul acceleration using Intel® NIC, a fronthaul appliance on the Intel® Arria® 10 FPGA SoC development kit, and a RoE to CPRI connection or a legacy radio.

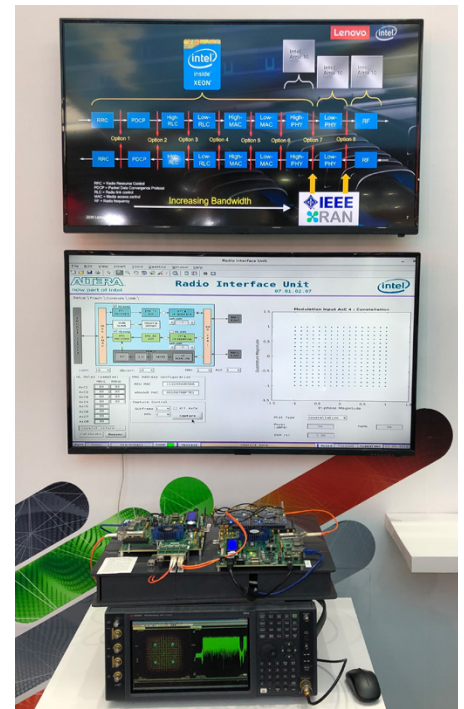


Figure 6. Mobile World Congress (MWC) 2018 Shanghai demo

FPGA IP portfolio for fronthaul

Intel offers a wide portfolio of options for implementing flexible and efficient fronthaul interfaces.

KEY FPGA IP OFFERINGS

Common Public Radio Interface (CPRI) IP	Intel has been supporting the CPRI IP for many years. Intel supports the latest version of the classic CPRI protocol specification v7.0 released in October 2015 across different device families with support for different line rates. Learn more.
eCPRI IP	Intel is developing an eCPRI IP v1.2-compliant IP, which is planned for release in 2019 with a road map for eCPRI v2.0. The new 2.0 specification will enhance support for 5G fronthaul by providing functionality to support CPRI (7.0) over Ethernet allowing for CPRI and eCPRI interworking.
Radio over Ethernet (RoE) IP	Intel has been on the standardization-driving seat of IEEE1914.3 for many years and provides a full reference design implementation of the 2018 release of IEEE1914.3 RoE. This reference design runs on the Intel® Arria® 10 FPGA SoC development kit, takes a 10 GbE RoE interface-carrying frequency domain IQ on one side, implements the frequency to time domain functionality (IFFT/FFT and cyclic prefix addition/removal and PRACH), and provides either 2x4.9252 Gbps or 2x9.8304 Gbps CPRI interface connectivity on the other side.
Compression decompression IP	Mu-Law and block floating-point compression and decompression IP cores are available from Intel and are compliant with the xRAN specification v2.0.
xRAN IP plans	Early release Q4 2018; fully compliant release Q2 2019.
Synchronization and 1588 IP	While Ethernet-based fronthaul allows for greater vendor interoperability and the use of white-box Ethernet switches, CPRI inherently provides high-quality time and frequency accuracy. In order to achieve a similar level of accuracy with Ethernet, either a GNSS conditioned clock or high-quality software protocol solution is required. The precision time protocol (PTP), IEEE1588v3, IEEE802.1AS, and ITU-T G.8273.2 specifications come into play here. These standards provide a framework for fixing the timing accuracy challenges.
Channel coding	Turbo, LDPC, and Polar channel coding including rate (de)matching, and (de)interleaving are available.
OFDMA generation	iFFT/FFT, cyclic prefix addition/removal, and PRACH processing functions.
Channel estimation	Channel estimation MIMO processing algorithms including MMSE, MLD, and others are also available.

Moving forward

Network traffic has grown 250,000 percent in little more than a decade.¹ 5G has the potential to radically transform our digital experience yet again. Intel works closely with standards bodies, such as the ORAN Alliance, and offers enabling technologies to help ensure the communications industry can adapt, grow, and respond to the opportunities ahead.



1. http://about.att.com/newsroom/2017_network_predictions.html

Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit [intel.com/benchmarks](https://www.intel.com/benchmarks). Performance results are based on testing as of October 2018, and may not reflect all publicly available security updates. See configuration disclosure for details. No product can be absolutely secure.

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