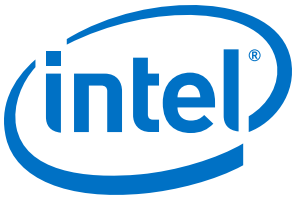

AN 848: Implementing Intel® Cyclone® 10 GX Triple-Rate SDI II with Nextera FMC Daughter Card Reference Design

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The triple-rate (up to 3G) Serial Digital Interface II (SDI II) parallel loopback with external voltage-controlled crystal oscillator (VCXO) reference design demonstrates the transmission and reception of video data using the SDI II Intel® FPGA IP core, Intel Cyclone® 10 GX FPGA development kit, and the Nextera FMC daughter card.

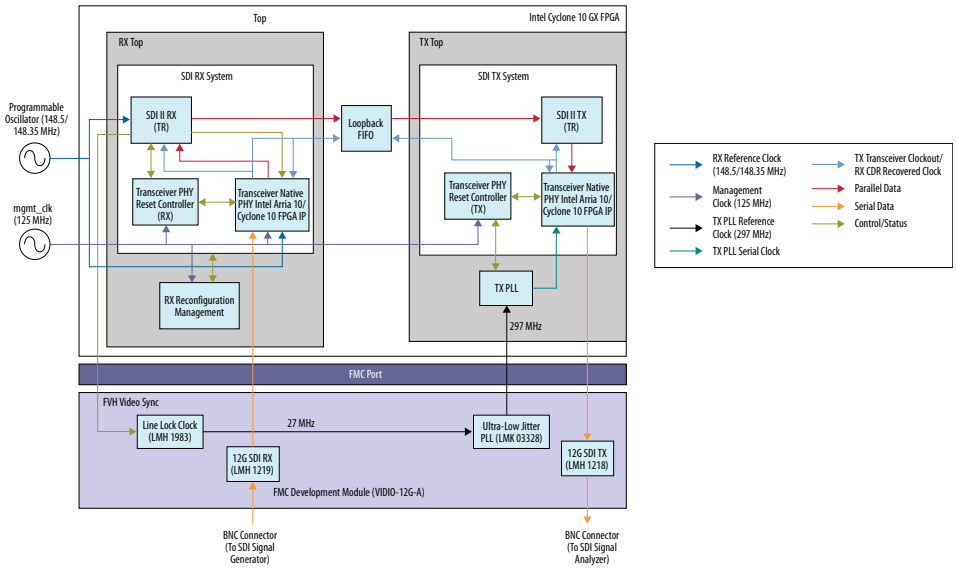
This application note provides quick steps to generate your design from the Intel Quartus® Prime Pro Edition software and implement your design using the Intel Cyclone 10 GX triple-rate SDI II with the Nextera FMC daughter card.

Related Information

- Intel FPGA SDI II Design Example User Guide for Intel Cyclone 10 GX Devices
- Intel Cyclone 10 GX FPGA Development Kit User Guide
- AN 848: Implementing Intel Cyclone 10 GX Triple-Rate SDI II with Nextera FMC Daughter Card Reference Design

Reference Design Block Diagram

Figure 1. Reference Design Simplified Block Diagram



Key Features

This reference design provides the following key features:

- A single-link transmission or reception of the SDI II video data at data rates up to 3 Gbps. The auto-detect and auto-switch features of the SDI II Intel FPGA IP core allow you to switch easily between the following triple-rate SDI II standards:
  - SD-SDI II at 270 Mbps
  - HD-SDI II at 1.485/1.4835 Gbps
  - 3G-SDI II at 2.97/2.967 Gbps
- A simplex TX channel and a simplex RX channel. Each channel has its own design components. For more information, refer to the *Design Components* section.
  - TX channel design components:
    - Transceiver Native PHY IP core in TX simplex mode
    - SDI II transmitter
    - TX channel transceiver PHY reset controller
    - TX PLL with 297-MHz reference clock
  - RX channel design components:
    - Transceiver Native PHY IP core in RX simplex mode
    - SDI II receiver
    - RX channel transceiver PHY reset controller
    - RX reconfiguration management
- Tune the TX reference clock using the F-sync, V-sync, and H-sync input reference timing signals sourced from the SDI II Intel FPGA IP receiver. A 27-MHz clock is generated from the FVH video sync and is feed into the ultra-low jitter PLL (LMK 03328). The LMK 03328 generates a 297/296.70-MHz output for the TX PLL reference clock at the FPGA.

Related Information

Design Components on page 5

Design Components

Table 1. Reference Design Components

Design Components	Description
SDI II Intel FPGA IP core	• TX—receives the video data from the top level and encodes the necessary information (for example, line number (LN), cyclic redundancy check (CRC), payload ID) into the data stream. • RX—receives the parallel data from the Transceiver Native PHY Intel FPGA IP core and decodes the necessary information (for example, descrambling, realigning data).
Transceiver Native PHY for Intel Arria® 10/Cyclone 10 FPGA IP core	• TX: — Hard transceiver block that receives parallel data from the SDI II Intel FPGA IP core and serializes the data before transmission. — **Enable the simplified data interface** option—connects the parallel data directly to the `tx_dataout` signal of the SDI II Intel FPGA IP core. • RX: — Hard transceiver block that receives serial data from an external video source. — **Enable the simplified data interface** option—connects the parallel data directly to the `rx_datain` signal of the SDI II Intel FPGA IP core.
Transceiver PHY Reset Controller Intel FPGA IP core	• TX: — The reset input of this controller is triggered from the top level. — The controller generates the corresponding analog and digital reset signal to the Transceiver Native PHY Intel Cyclone 10 GX FPGA IP core, according to the reset sequencing inside the block. — Use the `tx_ready` output signal from the block as a reset signal to the TX core to indicate that the transceiver is up and running, and ready to receive data from the core. • RX: — The reset input of this controller is triggered by the SDI II Intel FPGA IP core. — The controller generates the corresponding analog and digital reset signal to the Transceiver Native PHY Intel Cyclone 10 GX FPGA IP core, according to the reset sequencing inside the block.

continued...

Design Components	Description
TX PLL	Transmitter phase-locked loop (PLL) block that provides the serial fast clock to the Transceiver Native PHY Intel Cyclone 10 GX FPGA IP core. This reference design uses the Transceiver CMU PLL Intel Cyclone 10 GX FPGA IP core.
RX Reconfiguration Management	RX transceiver reconfiguration management block that reconfigures the Transceiver Native PHY Intel Cyclone 10 GX FPGA IP core to receive different data rates from SD-SDI to 3G-SDI standards.
Loopback FIFO	This block contains a dual-clock FIFO (DCFIFO) buffer to handle the data transmission across asynchronous clock domains—the receiver recovered clock and transmitter clock out. • The receiver sends the decoded RX data to the transmitter through this FIFO buffer. • When the receiver locks, the RX data is written to the FIFO buffer. • The transmitter starts reading, encoding, and transmitting the data when half of the FIFO buffer is filled.

Requirements

Hardware Requirements

The reference design requires the following hardware tools:

- Intel Cyclone 10 GX FPGA Development Kit (10CX220YF780E5G)
- SDI Signal Generator
- SDI Signal Analyzer
- Bayonet Neill-Concealman (BNC) to BNC cables
- VIDIO™ FMC Development Module VIDIO-12G-A (Nextera 12G SDI FMC daughter card)

Software Requirements

The reference design requires the following software:

- Intel Quartus Prime Pro Edition version 18.0
- Intel Cyclone 10 GX FPGA Development Kit Board Test System

Related Information

Intel Cyclone 10 GX FPGA Development Kit Board Test System

Reference Design Walkthrough

Running the Reference Design

To run the reference design, follow these steps:

1. Compile the project.
2. Setup the hardware.
3. Configure the FPGA.
4. Check the video formats and jitter reading.

Compiling the Project

Note: You can also customize the reference design generated by the SDI II Intel FPGA IP core to meet your design requirements. For more information, refer to the Customizing the Reference Design on page 12.

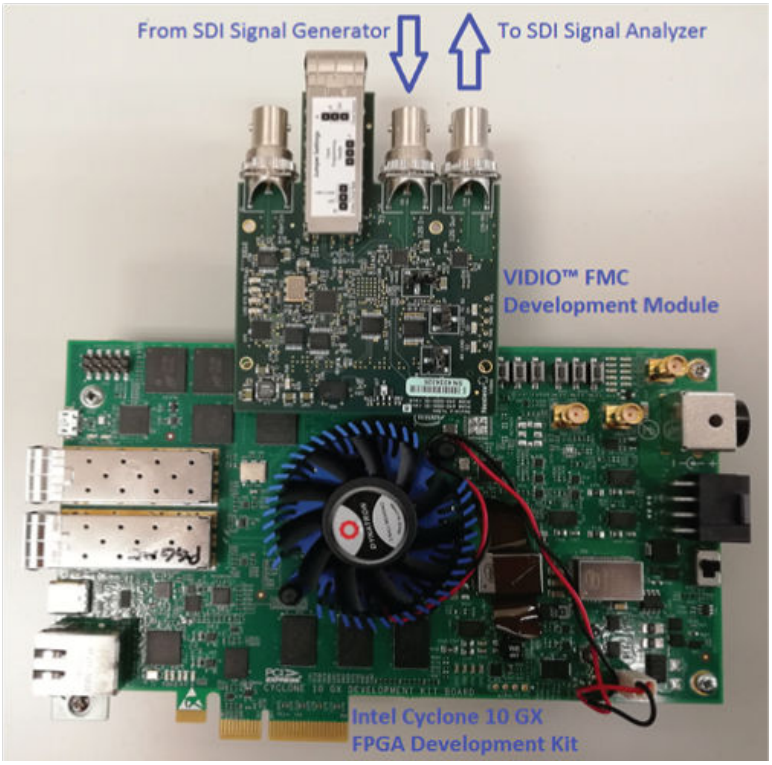
To download the reference design from the Design Store, follow these steps:

1. To test the reference design targeted for the Intel Cyclone 10 GX device, download the reference design file to your local project directory.
2. Launch the Intel Quartus Prime Pro Edition software.
3. To prepare the design template in the Intel Quartus Prime Pro Edition software GUI, click **File>Open** and change the file type to the Intel Quartus Prime Design Template File (*.**par**). Browse to the **.par** file and click **OK**.

To compile the project, select **Processing>Start Compilation**.

Setting up the Hardware

Figure 2. Intel Cyclone 10 GX FPGA Development Kit and Nextera 12G SDI FMC Daughter Card



For the hardware setup to run the reference design, follow these steps:

1. Connect the Nextera 12G SDI FMC daughter card to the FMC port on the Intel Cyclone 10 GX FPGA Development Kit. For more information, refer to the *Intel Cyclone 10 GX FPGA Development Kit and Nextera 12G SDI FMC Daughter Card* figure.
2. Set the remaining DIP switches to the default factory settings. For more information, refer to the *DIP Switch Settings* table in the *Intel Cyclone 10 GX FPGA Development Kit User Guide*.
3. Connect the Nextera daughter card BNC RX connector (J1/12G IN) to the SDI Signal Generator and the Nextera daughter card BNC TX connector (J2/12G OUT) to the SDI Signal Analyzer.
4. Connect the USB cable to the Micro USB Blaster connector on the development kit.
5. Connect the power adapter (packaged together with the development board) to the power supply jack.
6. Turn on the power for the Intel Cyclone 10 GX FPGA Development Kit. The hardware system is now ready for programming.
7. Complete the following steps to configure the output clock frequencies of the programmable clock generator (Si5332) used in the reference design:
   a. Download and unzip the `Kit Collateral.zip` design package from the *Intel Cyclone 10 GX FPGA Development Kit* web page.

b. Launch the Intel Quartus Prime Pro Edition software and then run the `Clock Controller.exe` application from the `cyclone-10-gx-kit-collateral\examples\board_test_system` directory.

c. Set the OUT1 frequency to **148.5 MHz** and the OUT6 frequency to **125 MHz** on the **Si5332(U64)** tab. For more information, refer to the *Clock Controller GUI for Si5332* figure.

d. Close the `Clock Controller` application.

Figure 3. Clock Controller GUI for Si5332

8. To switch between the fractional frame rate and integer frame rate video formats, follow these steps:

a. Change the jumper (J8) position on the Nextera 12G-SDI FMC daughter card based on the setting in the *Jumper Settings for Switching between PAL and NTSC*. For more information, refer to the *Jumper Settings on the Nextera 12G-SDI FMC Daughter Card* figure.

b. Press the push button (PB1) on the Intel Cyclone 10 GX FPGA Development Kit to trigger a power cycle to the LMK03328 on the Nextera 12G-SDI FMC daughter card every time you change the jumper (J8) position.

Figure 4. Jumper Settings on the Nextera 12G-SDI FMC Daughter Card

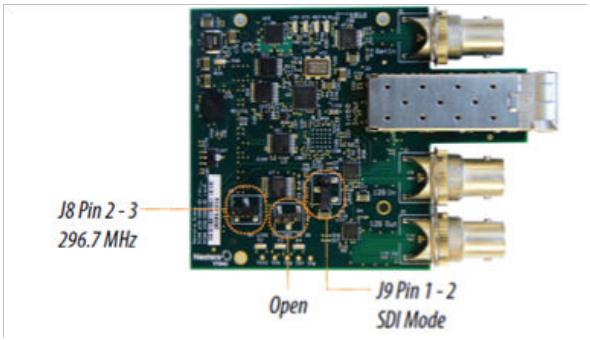


Table 2. Jumper Settings for Switching between PAL and NTSC

Jumper Block	Setting	Description
J7	—	Programming header.
J8	• 1–2 for PAL • 2–3 for NTSC	To switch frequency between PAL and NTSC for the TX channel: • Pin 1–2 = 297 MHz • Pin 2–3 = 297/1.001 MHz
J9	1–2	To select the SDI or IP mode: • Pin 1–2 = SDI mode • Pin 2–3 = IP mode

Related Information

- Intel Cyclone 10 GX FPGA Development Kit
- Default Switch and Jumper Settings
  Provides more information on the DIP switch settings.

Configuring the FPGA

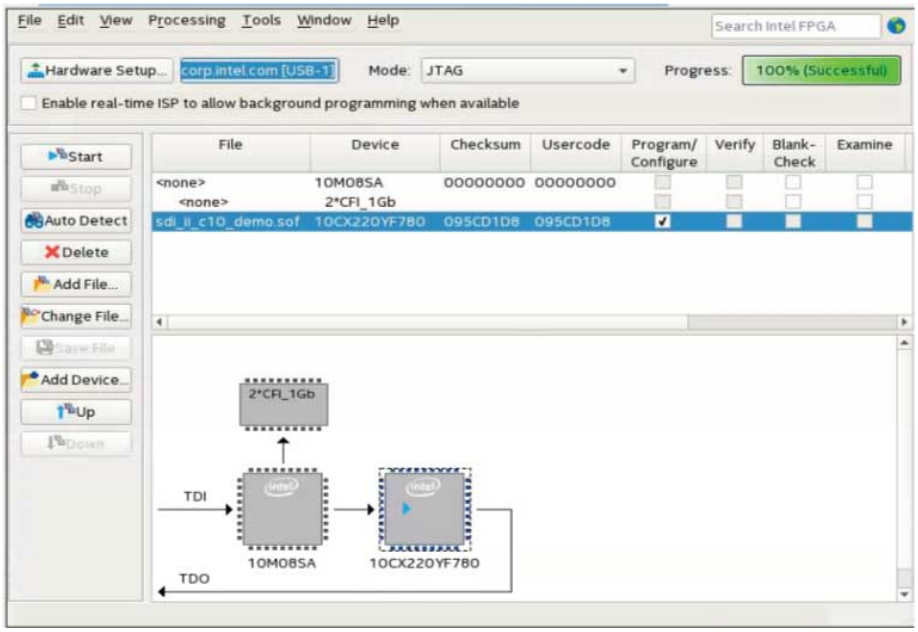
Before configuring the FPGA, ensure the following tasks are completed:

- The Intel FPGA Download Cable II driver is installed on the host computer
- The Intel Cyclone 10 GX FPGA Development Kit is powered on
- No other running application is using the JTAG chain

To configure the FPGA, follow these steps:

1. In the Intel Quartus Prime Programmer, select **Hardware Setup>USB-Blaster II [USB-1]**.
2. Click **Auto Detect** to display the devices in the JTAG chain. Select **10M08SA** for device 1 and **10CX220Y** for device 2.
3. Right click **10CX220Y** and select **Change File**. Choose the appropriate SRAM Object File (**.sof**) from the `/quartus` directory. Click **Open**.
4. Turn on **Program/Configure** for the **.sof** file.
5. Click **Start** to program the image into the FPGA.

Figure 5. Intel Quartus Prime Programmer



Checking the Video Formats and Jitter Reading

Generate different video patterns to the SDI RX using the SDI Signal Generator and check the video patterns displayed on the SDI Signal Analyzer. If the design is working correctly, the SDI Signal Analyzer should display the same video pattern as the SDI Signal Generator.

You must ensure the jitter reading displayed on the SDI Signal Analyzer meets the Society of Motion Picture and Television Engineers (SMPTE) specification.

Customizing the Intel Quartus Prime Pro Edition Reference Design

The following sections provide an example on how to customize the Intel Cyclone 10 GX triple-rate SDI II reference design for implementation on the Intel Cyclone 10 GX development kit with the Nextera 12G-SDI FMC daughter card.

Note: You may skip this section if you are downloading the reference design directly from the design store.

Generating the Reference Design

Follow these steps to generate the reference design:

1. Launch the Intel Quartus Prime Pro Edition software.
2. Create a project and select your Intel Cyclone 10 GX device.
3. In the **IP Catalog**, select **SDI II Intel FPGA IP**. The **New IP Variant** window appears.
4. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named **<your_ip>.ip**.

5. Click **Create**. The parameter editor appears.
6. On the **IP** tab, select the following settings:
   a. Select **Triple rate (up to 3G-SDI)** for the video standard option.
   b. Select **Transmitter** or **Receiver** for the direction option.
7. On the **Design Example** tab, select the following settings:
   a. Select **Parallel loopback with external VCXO** for the select design option.
   b. Select **CMU/fPLL** for the TX PLL type option.
   c. Select **Synthesis** checkbox for the design example files option.
   d. Select **Verilog** for the generate file format option.
   e. Select **Custom Development Kit** for the select board option.
8. Click **Generate Example Design**.

Customizing the Reference Design

In the Intel Quartus Prime Pro Edition software, follow these steps:

1. Assume your design uses a 125-MHz clock for both the TX and RX Avalon®-MM interfaces for the reconfiguration and PHY reset controller blocks. Follow these steps to change the clock from 100 MHz to 125 MHz.
   a. Change the explicit clock rate for the following Clock Bridge components to 125000000.

      `reconfig_clk` and `rx_phy_rst_ctrl_clk` (located in the `sdi_rx_sys.qsys`)

      `tx_phy_rst_ctrl_clk` (located in the `sdi_tx_sys.qsys`)

   b. Change the input clock frequency for the TX and RX Transceiver PHY Reset Controller Intel FPGA IP to 125 MHz. The related components are:

      `rx_phy_rst_ctrl` (located in the `sdi_rx_sys.qsys`)

      `tx_phy_rst_ctrl` (located in the `sdi_tx_sys.qsys`)

      Note: You must double click on each component to open it in the parameter editor before you can change the value. You can skip this step if you use a 100-MHz clock for both the TX and RX Avalon-MM interfaces for the reconfiguration and PHY reset controller blocks.
2. The reference design uses a 297-MHz TX PLL reference clock. Follow these steps to change the TX PLL reference clock.
   a. Open the `tx_pll.ip` (located at `/rtl/tx/` directory).
   b. Change the PLL reference clock frequency to 297 MHz.
   c. Click **Generate HDL** button and then **Generate** button to generate the HDL design files for synthesis.
3. The `{usb_refclk_p}` is renamed to `{fmc_gbtclk_m2c_p0}` in the top-level file of this reference design. The `{c10_refclk_2_p}` is renamed to `{c10_refclk_1_p}` in the top-level file of this reference design.
4. Update the clock constraints in `sdi_ii_c10_demo.sdc`:
   a. Remove the following:

```
create_clock -period "100 MHz" -name{c10_refclk_2_p}
{c10_refclk_2_p}

create_clock -period "148.5 MHz" -name{usb_refclk_p}
{usb_refclk_p}
```

b. Add the following:

```
create_clock -period "125 MHz" -name {c10_refclk_1_p}
{c10_refclk_1_p}

create_clock -period "297 MHz" -name {fmc_gbtclk_m2c_p0}
{fmc_gbtclk_m2c_p0}
```

5. The reference design generated is not targeted on any development kit. You will need to manually assign your pin assignments. The following are the example pin assignments used in the reference design created using the Intel Cyclone 10 GX Development Kit.

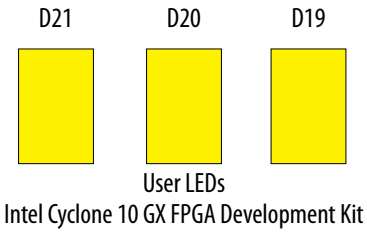
Table 3. Reference Design Pin Assignments for Intel Cyclone 10 GX Development Kit

Signal	Direction	Pin Location	Description
c10_refclk_1_p	Input	PIN_AB16	125-MHz clock for reconfiguration in the Avalon-MM interfaces.
sfp_refclk_p	Input	PIN U24	RX transceiver reference clock and SDI RX core clock.
fmc_gbtclk_m2c_p0	Input	PIN_W24	297-MHz TX PLL reference clock from the Nextera daughter card.
user_pb [0]	Input	PIN_AE4	Push button for the LEDs to switch between displaying the rx_std or rx_lock status.
user_pb [1]	Input	PIN_AD4	Push button to power down LMK03328 after switching the jumper settings.
user_pb [2]	Input	PIN_AH2	Push button for global reset.
user_led[3..0]	Output	PIN_AC7, PIN_AC6, PIN_AE6, PIN_AF6	Green LED display.
fmc_dp_m2c_p2	Input	PIN_AB26	SDI RX serial data from the FMC port.
fmc_la_tx_p1	Input	PIN_L1	RX cable equalizer lock status on the Nextera daughter card.
fmc_dp_c2m_p0	Output	PIN_AG28	SDI TX serial data from the FMC port.
fmc_la_tx_p12	Output	PIN_W4	Initialize LMH1983 on the Nextera daughter card.
fmc_la_tx_n12	Output	PIN_Y4	F-sync signal for LMH1983 on the Nextera daughter card.
fmc_la_tx_p14	Output	PIN_T4	V-sync signal for LMH1983 on the Nextera daughter card.
fmc_la_tx_n14	Output	PIN_U5	H-sync signal for LMH1983 on the Nextera daughter card.
fmc_la_tx_p15	Output	PIN_U6	Power-down signal for LMH1983 on the Nextera daughter card.

Viewing the Results

Monitor User LEDs

Figure 6. User LEDs



This test uses the following LEDs to indicate the respective conditions.

Table 4. User LEDs

The User LEDs indicate the expected results. A logical 1 indicates that the LED illuminates and a logical 0 indicates otherwise.

User LEDs	Results	
	PB0 = ON	PB0 = OFF
D19	The standard of the RX signal video: • SD: [D21, D20, D19] = 000 • HD: [D21, D20, D19] = 001 • 3Gb: [D21, D20, D19] = 010 • 3Ga: [D21, D20, D19] = 011	Illuminates when the `frame_locked` signal is asserted.
D20		Illuminates when the `trs_locked` signal is asserted.
D21		Illuminates when the `aligned_locked` signal is asserted.

Verify the Video Image and Jitter Results at the Signal Analyzer

The following figures show examples of video image and jitter results at the signal analyzer with different input video formats for 3G-SDI, HD-SDI, and SD-SDI.

Figure 7. Video Image and Jitter Result for Video Format 1920 x 1080i 59.94 Hz

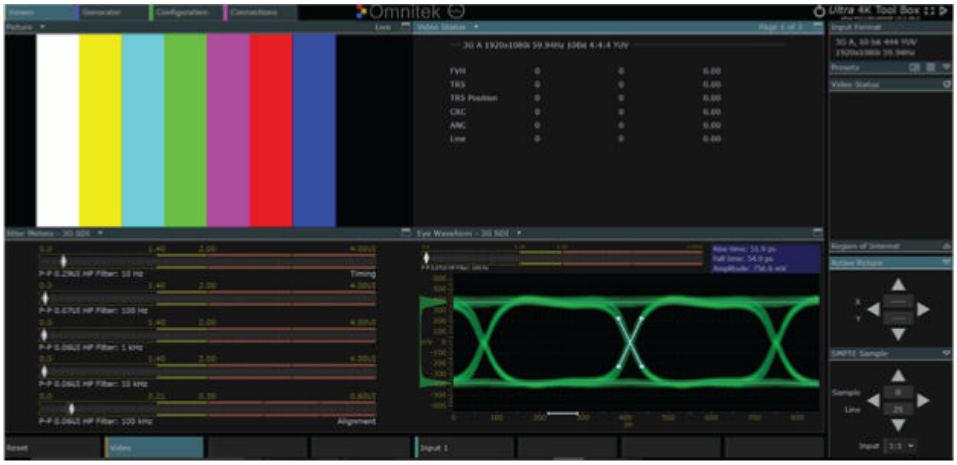
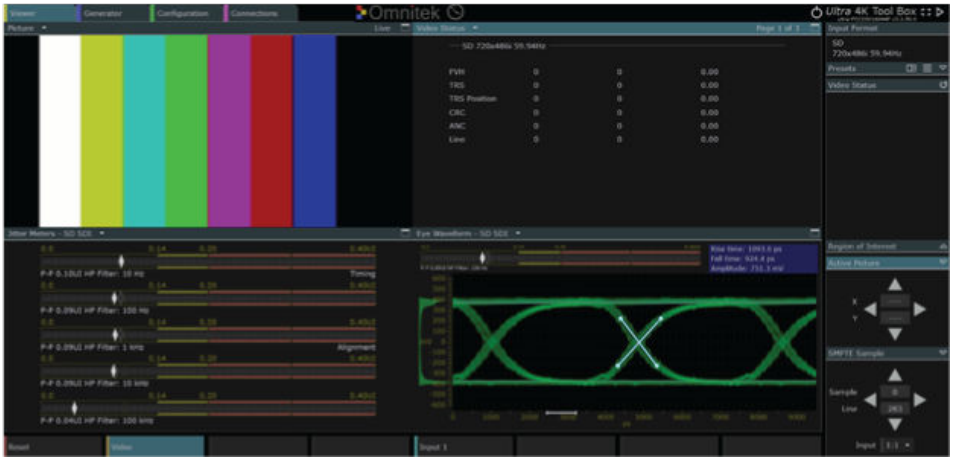


Figure 8. Video Image and Jitter Result for Video Format 1920 x 1080i 50 Hz

Figure 9. Video Image and Jitter Result for Video Format 1280 x 720p 29.97 Hz

Figure 10. Video Image and Jitter Result for Video Format 720 x 486i 59.94 Hz



Document Revision History for AN 848: Implementing Intel Cyclone 10 GX Triple-Rate SDI II with Nextera FMC Daughter Card Reference Design

Document Version	Intel Quartus Prime Version	Changes
2018.07.05	18.0	Initial release.