# Enpirion® Power Application Note #103

## Compensating with High Output Capacitance for Altera's Enpirion Point of Load Synchronous Buck Converters with Integrated Inductor

## Summary

This application note explains the voltage mode control mechanism for Altera Enpirion products and provides a brief tutorial on how to compensate with high output capacitance for Altera's Enpirion point of load synchronous buck converters. Examples for EN63xx products will also be provided for a better understanding of the method to adjust the loop compensation.

## Introduction

All of Altera Enpirion products have been designed for operating at certain minimum amount of input and output capacitance. The one question customers often ask is:"What is the maximum amount of output capacitance Altera Enpirion products can support without having any stability issues?" Customers often put a fairly large number of capacitors at the output of Altera Enpirion converters for the purpose of reducing ripple, reducing load transient deviation, or even the load manufacturer's requirement. When these customers add the extra output capacitors without further analysis or testing, stability problems may occur. Fortunately, the system can be stabilized easily with some minor change of the external compensation components.

## The Compensation Network

Figure 1 shows the closed loop system with a Type III compensation network for most of Altera Enpirion synchronous buck converters. The gray area represents the converter internal circuit which includes an advanced integrated inductor, integrated MOSFETs, driver circuit, a PWM comparator, and internal compensation.

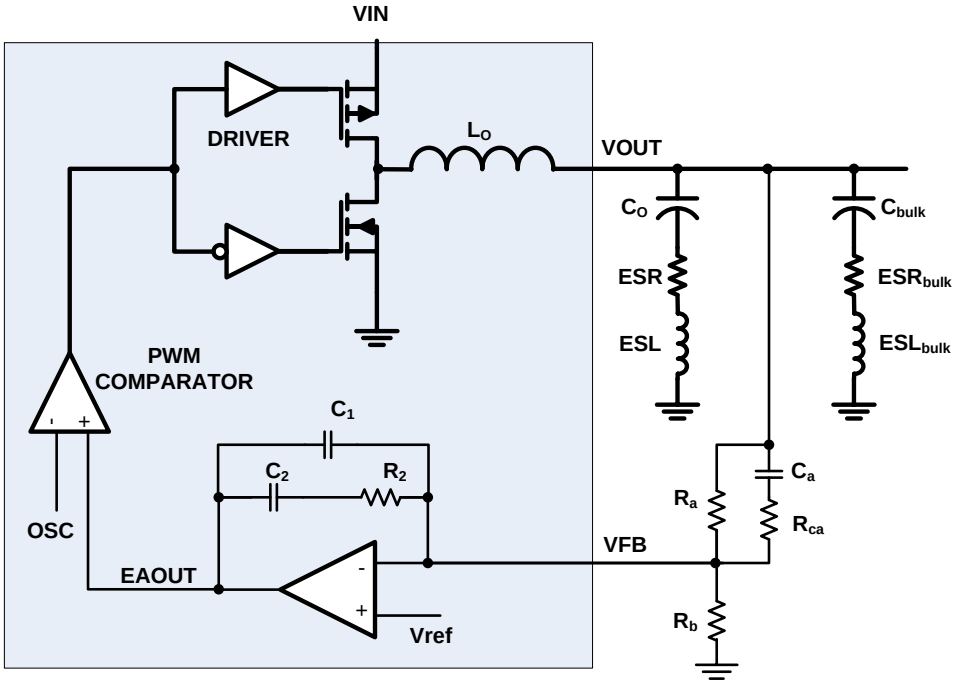



**Figure 1. Closed Loop System with TYPE III Network**

Without considering the extra bulk capacitors that the customers added, the output filter consists of the internal inductor $L_O$ and external recommended output capacitor $C_O$. The following equation shows the transfer function of the output filter.

$$GAIN_{filter} = \frac{1 + s \cdot ESR \cdot C_O}{1 + s \cdot ESR \cdot C_O + s^2 \cdot L_O \cdot C_O}$$

The transfer function of the output filter shows the well known double pole, the DC resistance (DCR) of the inductor and the Equivalent Series Resistance (ESR) of the capacitor provide the damping factor of this resonant circuit. Due to the very high switching frequency of Altera Enpirion products, the Equivalent Series Inductance (ESL) also plays an important role in the system design, it forms double zero with output capacitance. For simplicity, we only consider the single zero as a function of output capacitance and its ESR in the transfer function.

A TYPE III compensation network is utilized to compensate the system. The compensation network includes internal error amplifier, $C_1$, $C_2$, $R_2$ and external components, $R_a$, $C_a$, $R_{ca}$.

$$GAIN_{TYPEIII} = \frac{R_a + R_{ca}}{R_a \cdot R_{ca} \cdot C_a} \cdot \frac{\left(s + \frac{1}{R_2 C_2}\right) \cdot \left(s + \frac{1}{(R_a + R_{ca}) C_a}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_a C_a}\right)}$$

The Type III network utilizes two zeros to give a phase boost of 180°. This boost is necessary to counteract the phase drop of the output filter at the double pole. Figure 2 shows the asymptotic Bode gain plot for the Type III compensated system and the locations of zeros and poles.

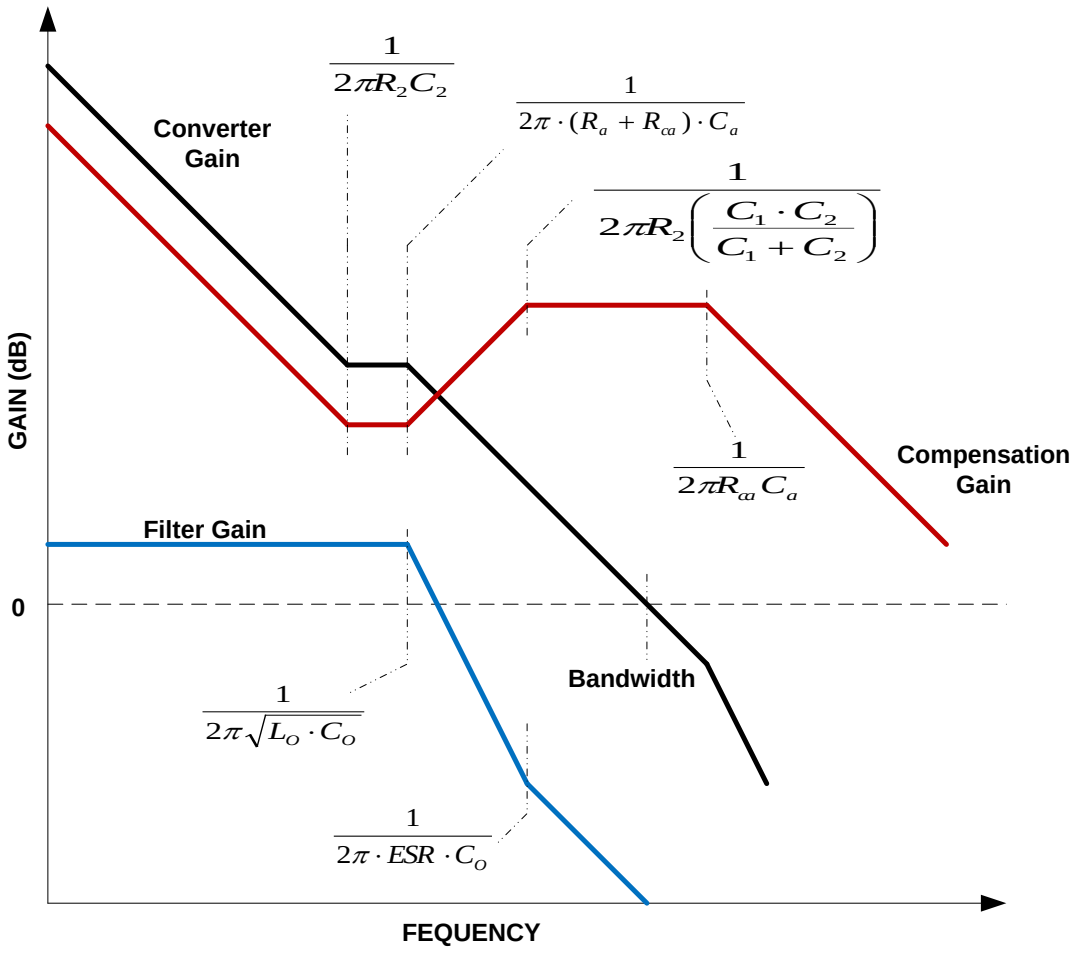



**Figure 2. TYPE III Compensated Network**

For Altera's Enpirion converter products, the external resistor Ra is not only part of the resistor divider to set the output voltage, but also part of the compensation network. Its value significantly affects the loop gain, loop bandwidth and the phase margin. Moreover, there is no $R_{ca}$ in the compensation network for some of Altera Enpirion converters. For those converters, the last pole in Figure 2 is generated by the intersection of compensation gain and error amplifier open loop gain. We will not get into the details, interested readers can refer to Abu-Alfotouh's paper for detailed information (*APEC2007, pp736-742*).

## Compensating with extra high output capacitance

The double pole of the output filter is around $1/2\pi\sqrt{L_O \cdot C_{out}}$, where $C_{out}$ is the equivalent capacitance of all the output capacitors including the minimum required output capacitors that Altera recommended and the extra bulk capacitors customers added based on their design requirement. While the compensation network was designed based on the capacitors that Altera recommended, increasing the output capacitance will shift the double pole to the direction of lower frequency, which will lower the loop bandwidth and phase margin. In most cases, it won't cause the stability problem if the extra output capacitance is not too high, since Altera's Enpirion converter has adequate phase margin to accommodate some extra output capacitance. But when the extra output capacitance is higher than a couple of hundred of microfarads, the zero also need to shift to lower frequency to counteract the phase drop due to the double pole shifting to lower frequency. This can be easily implemented by increasing the leading capacitor value, Ca. In addition the ESR of the output capacitors also helps since the ESR and output capacitance forms a zero which also helps to boost the phase, although ESR is not favorable to low output voltage ripple.

The legitimate question is how much capacitance should one increase the leading capacitor? There is no easy equation to calculate the value, the best way to do is to perform an AC small signal simulation or make the actual loop measurement using frequency analyzer. The problem is that most customers don't have the ability to simulate the loop or measure the bode plot. Fortunately there is a simple way to check the system stability to the extent of first order approximation by measuring the load transient performance. Figure 3 is the theoretical close-loop unit-step response for various phase margins (φ). The transient response for small phase margin exhibits sinusoidal-type waveforms with decaying amplitude. The exact load transient response of the converter may differ from the plots of Figure 3, because of the additional poles and zeroes in the system loop, because of differences in initial conditions, load step slew rate, etc. Nonetheless, Figure 3 illustrates how small phase margin lead to overshoot and ringing. We normally require the phase margin is higher than 45°C.

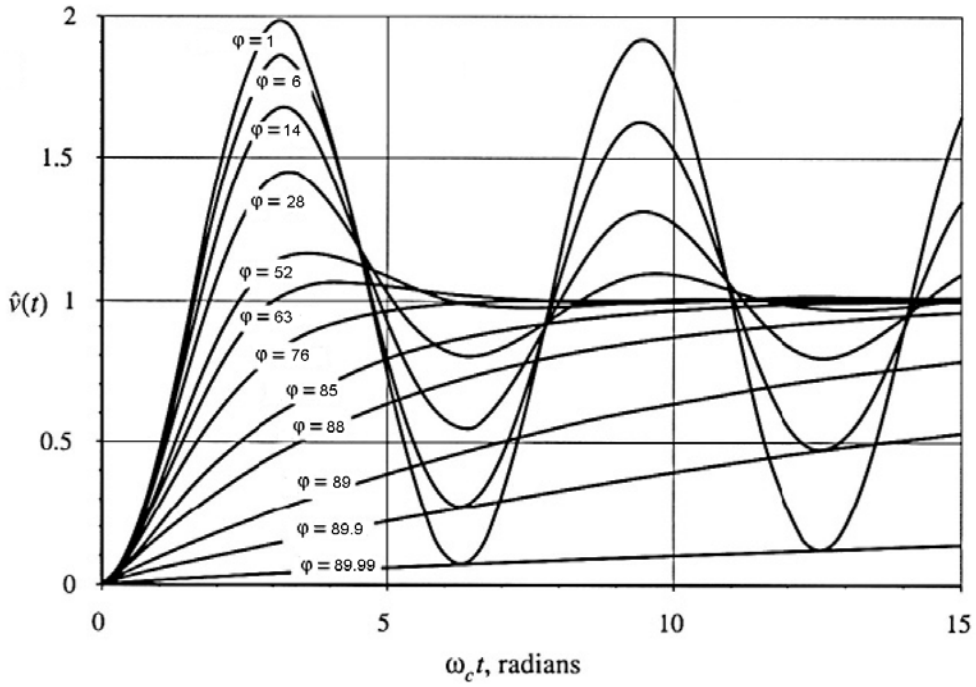



**Figure 3. Unit-step response of the second-order system**

Figure 4 shows the simulated load transient response and its corresponding Bode plots at different output and leading capacitors for EN6347.

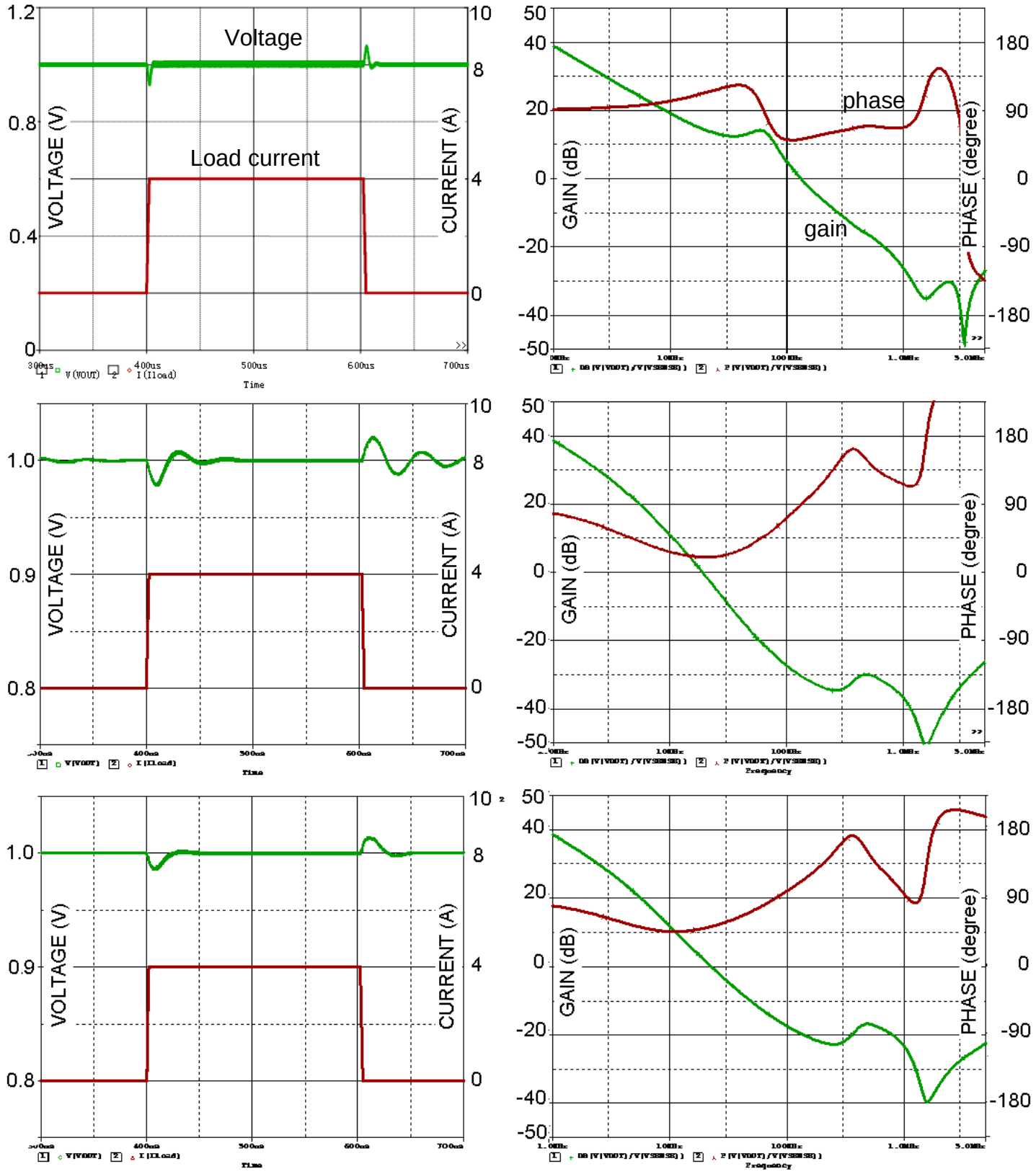



**Figure 4. EN6347 load transient response and bode plots, top row: using Altera recommended output capacitors ($C_{out}$=47*µF*+10*µF*) and leading capacitor ($C_a$=10pF); middle row: $C_{out}$=47*µF*+10*µF*+1*mF*, $C_a$=10*pF*; bottom row: $C_{out}$=47*µF*+10*µF*+1*mF*, $C_a$=39*pF***

Top row shows the load transient and bode plot using Altera recommended output capacitors, 47*µF* in parallel with 10*µF*, and leading capacitor, 10*pF*. From the bode plot, we can read that the loop bandwidth is around 130*KHz*, the phase margin is about 52 degree. This is considered stable, so there is no ringing for the load transient response. The middle row shows the same load transient and bode plot under the same condition except add one 1000*µF* extra bulk capacitor at the output. Due to the double pole shifting to lower frequency, the phase drops occur at lower frequency, the loop bandwidth reduce to 20*KHz*, the phase margin is only about 20. The load transient shows the ringing as the consequence of low phase margin. In order to stabilize the loop, the compensation network needs to be adjusted to boost the phase to above 45 degree. By increasing leading capacitor, $C_a$, to 39*pF*, the Zero formed by Ra, Rca and Ca is also shifting to lower frequency, which can counteract the phase drop due to extra bulk capacitors. The bottom row shows the result, phase margin goes back to 52, the bandwidth increases to 24*KHz*, and the ringing of load transient disappeared.

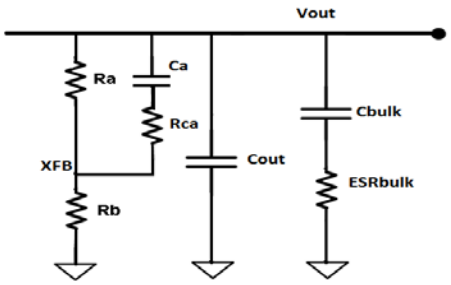
Since ESR helps boost the phase margin for the control loop, there may be some minimal ESR requirement for any bulk capacitance to be added to the output of the Altera Enpirion devices. Please contact Altera Power Applications support for details regarding specific use cases.

The following guidelines summarize the steps to experimentally adjust the compensation components when extra bulk capacitors are added at the converter output based on lab measurements:

1. First check the load transient performance using Altera recommended output capacitors and compensation components; make sure there is no ringing or oscillation.
2. Put the extra bulk capacitor at the converter output, check the load transient performance, look for ringing or sign of ringing.
3. If there is any sign of ringing, increase $C_a$ in 20% step until the ringing go away.
4. Measuring Bode plot using frequency analyzer is the best way to check the system stability, please contact Altera Power Applications if you need further technical support.

## Examples to handle the extra bulk capacitors

The following gives the compensation adjustment for Altera Enpirion EN63xx series products.




1. EN6337: (Cout=47uF+10uF, Ra=200K, Ca=15pF, Rca=0)

   - If 2x47uF ≤ $C_{bulk}$ ≤ 9x47uF
     i. $C_a$ need to be adjusted to 39pF
   - If 9x47uF(1206) <$C_{bulk}$≤ 1000uF
     i. $C_a$ need to be adjusted to 56pF
     ii. The minimum $ESR_{bulk}$ has to be greater than 4mΩ, where the $ESR_{bulk}$ includes ESR of bulk capacitor and the trace resistance between the sensing point and bulk capacitor.

2. EN6347: (Cout=47uF+10uF, Ra=200K, Ca=10pF, Rca=0)

   - If 2x47uF ≤ $C_{bulk}$ ≤ 5x47uF
     i. $C_a$ need to be adjusted to 27pF
   - If 5x47uF < $C_{bulk}$ ≤ 9x47uF
     i. $C_a$ need to be adjusted to 33pF

- If 9x47uF(1206) <$C_{bulk}$≤ 1000uF
    i. $C_a$ need to be adjusted to 47pF
    ii. The minimum $ESR_{bulk}$ has to be greater than 4mΩ, where the $ESR_{bulk}$ includes ESR of bulk capacitor and the trace resistance between the sensing point and bulk capacitor.

3. EN6360: ($C_{out}$=2x47uf, $R_a$=48.4xVIN KΩ, $C_a$=3.83/$R_a$ uF, $R_{ca}$=15KΩ)
    - If 100uF ≤ $C_{bulk}$ ≤ 1000uF, the compensation do not need to be modified as long as the minimum $ESR_{bulk}$ is greater than 6mΩ.

4. EN63A0: ($C_{out}$=3x47uF, $R_a$=48.4xVIN KΩ, $C_a$=4.6/$R_a$ uF, $R_{ca}$=12KΩ)
    - If 100uF ≤ $C_{bulk}$ ≤ 1000uF, the compensation do not need to be modified as long as the minimum $ESR_{bulk}$ is greater than 6mΩ.

Contact Altera Power Applications support to see if your use cases require any minimum ESR for the bulk capacitor.

## Contact Information

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Phone: 408-544-7000
www.altera.com