Intel® Agilex™ I-Series SoC FPGA Product Table

PRODUCT LINE		AGI 019	AGI 022	AGI 023	AGI 027
Resources	Logic elements (LEs)	1,918,975	2,208,075	2,308,080	2,692,760
	Adaptive logic modules (ALMs)	650,500	748,500	782,400	912,800
	ALM registers	2,602,000	2,994,000	3,129,600	3,651,200
	High-performance crypto blocks	2	0	2	0
	eSRAM memory blocks	1	0	1	0
	eSRAM memory size (Mb)	18	0	18	0
	M20K memory blocks	8,500	10,900	10,464	13,272
	M20K memory size (Mb)	166	212	204	259
	MLAB memory count	32,525	37,425	39,120	45,640
	MLAB memory size (Mb)	20	23	24	28
	I/O PLL	10	16	10	16
	Variable-precision digital signal processing (DSP) blocks	1,354	6,250	1,640	8,528
	18 x 19 multipliers	2,708	12,500	3,280	17,056
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.4 / 4.9	9.4 / 18.8	2.4/4.9	12.8/25.6
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	240	360	240	360
	AIB interaces	4	4	4	4
	Memory devices supported	DDR4 and QDR IV			
	Secure data manager	AES-256/SHA-256 bitstream encryption or authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection			
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache , NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4			
Tile Resources	F-Tile	PCI Express(PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct			
	R-Tile	Compute Express Interface (CXL) - Link width x16 lanes, x8 lanes PCIe hard IP block (Gen5 x16) or Bifurcateable 2x PCIe Gen5 x8 (EP) or 4x Gen5 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO support Precise time management PIPE direct			

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F-Tile - Package Options and I/O Pins	Tile Configuration	GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) Channels			
3184B (56 mm x 45 mm, 0.92 mm Hex)	F-Tile x4		720(360) / 64(48) / 8(8)	480(240) / 64(48) / 8(8)	720(360) / 64(48) / 8(8)
F-Tile and R-Tile - Package Options and I/O Pins	Tile Configuration	GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ(116G PAM4) Channels / R- Tile 32G PCIe (CXL) lanes			
2957A (56 mm x 45 mm, 1.0 / 0.92 mm Hex)	F-Tile x1 & R-Tile x 3		720(360)/16(12)/4(4)/48(32)		720(360)/16(12)/4(4)/48(32)
3184A (56 mm x 45 mm, 0.92 mm Hex)	F-Tile x3 & R-Tile x1		720(360)/48(36)/8(8)/16(16)		720(360)/48(36)/8(8)/16(16)
1935A (42.5mm x 42.5mm, 1.025 mm Hex)	F-Tile x1 & R-Tile x 1	480(240)/16(12)/0(0)/16(16)		480(240)/16(12)/0(0)/16(16)	

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