

# Keeping pace with the ever-changing wireless landscape

Discover how to quickly adapt to the changing standards and evolving performance requirements of modern wireless communications with scalable silicon and platforms solutions from Intel.

## Q What's the challenge?

**A**

- Today's wireless infrastructure is built around heterogeneous networks comprised of many different-sized radios, ranging from Macro and Micro to Pico and up to Femto cells—see Figure 1.
- Each of these cells exhibits widely different requirements, including:
  - Number of bands (sub6GHz band: 600 MHz to 6GHz and millimeter wave band: 28GHz, 39GHz)
  - Technology (GSM, CDMA, UMTS, 4G LTE/LTE-A, 5G, NB-IOT)
  - Radio frequency (RF) output power level (typically 125 mW to 80 W per antenna element)
  - Number of antenna elements (typically up to 8 in Macro, 16-64 in mMIMO and to few hundreds in mmWave depending on EIRP coverage)
  - Number of carriers covering 4G, 5G, NB-IOT and legacy standards (2G, 3G)
  - Larger number of users per cell
  - Configuration (integrated antenna, remote radio head, traditional, active antenna arrays)
  - Form factor and power consumption (outdoor vs indoor with power over ethernet (PoE))

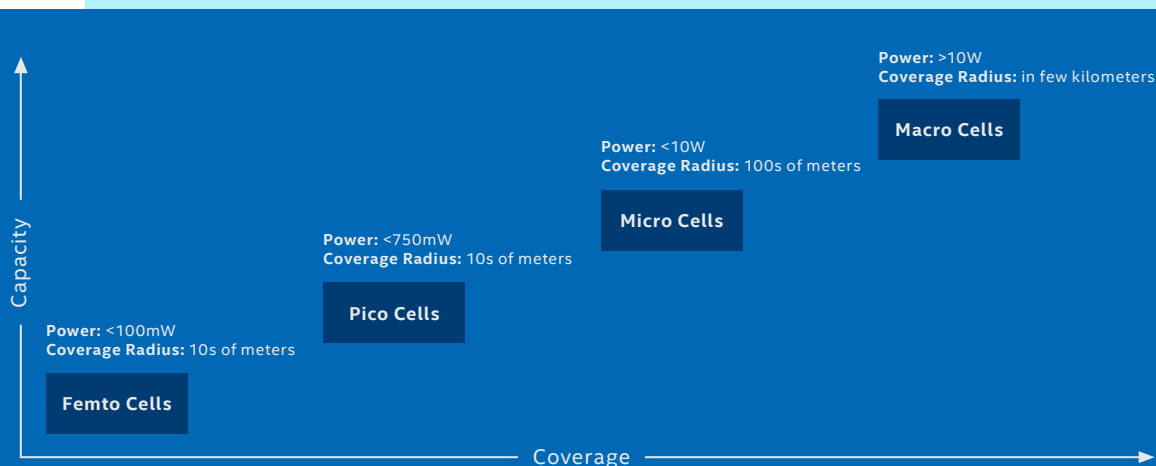


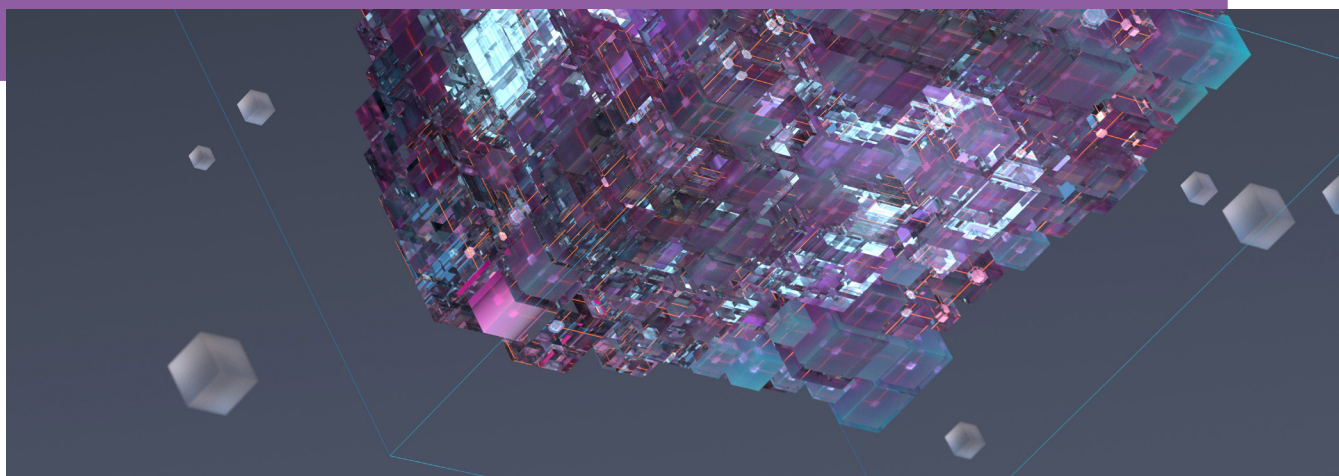
Figure 1. Different-sized radios, ranging from Macro and Metro to Pico and Femto cells.

## Q

## What's the solution?

## A

- To provide solutions for their networks, operators need to draw upon a broad range of radio hardware. Scalable platform solutions are desirable because they allow operators to quickly adopt to changing standards and to the evolving performance requirements characteristic of modern wireless communications.
- Equipment manufacturers desire scalable, flexible platform solutions to minimize design effort, cost, and time to market. Scalability also helps reduce test time and inventory and maximize design reuse.
- The key components of digital radio IP are fronthaul interface processing (CPRI/eCPRI/ORAN), Low Layer 1 (FFT/iFFT/PRACH/CP add/removal), digital up conversion (DUC), digital down conversion (DDC), crest factor reduction (CFR), and digital predistortion (DPD). Intel® Field Programmable Gate Arrays (Intel® FPGAs) and system-on-a-chip (SoC) devices provide a flexible, cost-effective, and scalable platform for implementing digital radios. New requirements and design fixes can be adopted rapidly and targeted at different radios. Intel also complements its FPGA offering with Intel® eASIC™ structured ASIC capability. eASIC technology is offering an ASIC-like cost and power reduction vehicle for high-volume production to address the challenges of radio heads including significantly improved thermals.
- Intel has partnered with various IP and hardware suppliers to deliver ORAN compliant O-RU reference platforms for Macro, Micro and Pico radio applications, and has a roadmap toward mMIMO and mmWave.
- Intel® Quartus® Prime Design Software includes DSP Builder for Intel FPGAs (Advanced Blockset). Leveraging MATLAB and Simulink, this tool allows engineers to design entire digital front ends in a system-level modeling environment and then target the Intel FPGA of their choice. Intel provides several advanced reference designs for radios including LL1, DUC/DDC and CFR.
- Intel Quartus Prime Design Software place and route tools are fully integrated, allowing designers to rapidly explore different implementation options to find the most efficient solution. Designs can be easily optimized to make the best use of the available resources and clock speeds.
- Intel Quartus Prime Design Software also includes Platform Designer. This top-level integration tool allows the designer to build their top-level design by connecting IP blocks, including DSP Builder for Intel FPGAs (Advanced Blockset), using Avalon® streaming and memory interfaces. From this point designers can construct a complete memory-mapped register file that can be directly interfaced to an internal SoC processor sub-system or external host.
- To further accelerate the design process, Intel also provides a multitude of hardware development kits, reference designs, and IP blocks.



## Learn More

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