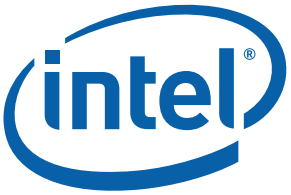


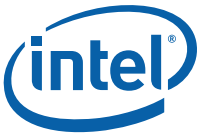
7th Generation Intel® Processor Family I/O for U/Y Platforms and 8th Generation Intel® Processor Family I/O for U Quad Core Platforms

Specification Update

August 2017

Revision 002

Document #: 334660-002



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Revision History

Revision	Description	Date
001	• Initial Release	August 2016
002	• Added support for 8th Generation Intel® Processor Family I/O for U Quad Core Platforms	August 2017

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
7th Generation Intel® Processor Families I/O for U/Y Platforms and 8th Generation Intel® Processor Families I/O f U Quad Core Platforms Datasheet – Volume 1 of 2	334658
7th Generation Intel® Processor Families I/O for U/Y Platforms and 8th Generation Intel® Processor Families I/O f U Quad Core Platforms Datasheet – Volume 2 of 2	334659

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so on).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata Summary

Erratum Number	Stepping	Status	ERRATA
	C1		
1	X	No Fix	xHC Data Packet Header and Payload Mismatch Error Condition
2	X	No Fix	USB SuperSpeed Packet with Invalid Type Field Issue
3	X	No Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
4	X	No Fix	Max Packet Size and Transfer Descriptor Length Mismatch
5	X	No Fix	xHCI Controller OC# Issue
6	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
7	X	No Fix	USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event
8	X	No Fix	USB 3.0 Devices Not Detected After Sx Resume
9	X	No Fix	PCI Express Unexpected Completion Status Bit May Get Set
10	X	No Fix	eSPI Concurrent Get-Config and Flash Cycles
11	X	No Fix	xHCI U3 Wake exit Issue
12	X	No Fix	xHCI controller USB Debug Port Disconnect Issue
13	X	No Fix	PSIC field incorrect value
14	X	No Fix	xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write
15	X	No Fix	SPI Dual I/O and Quad I/O Modes
16	X	No Fix	eSPI Turn Around (TAR) Spec Violation
17	X	No Fix	SMBus Transaction Using Memory Mapped I/O Registers
18	X	No Fix	xHCI Host Controller USB 2.0 Control Transfer may cause IN Data to be dropped
19	X	No Fix	System may hang while restoring HSIO ModPHY configuration
20	X	No Fix	xHCI Host Controller Reset May Cause a System Hang
21	X	No Fix	PCI Express* Gen2 x4 Device may cause a Machine Check Exception
22	X	No Fix	PCH PCIe* Controller Root Port Access Control Services Control Registers (ACSCTLR) Appear as Read Only
23	X	No Fix	Pull-up and Pull-down on SPI CS# and CLK Signals
24	X	No Fix	eSPI Error Reporting
25	X	No Fix	USB 3.0 DCI Control Packet issue
26	X	No Fix	eSPI Fatal Error Handling
27	X	No Fix	PCH PCIe* TX Pin State During L1.0 and L1.1 Substates
28	X	No Fix	Subsequent Deep S5 and S5 Exits Impacted After “Straight to S5 (Host Stays There)” Resets
29	X	No Fix	eSPI Bus Mastering

Specification Changes

Number	Stepping	SPECIFICATION CHANGES
	C1	
	X	There are no Specification Changes in this revision of the specification update.

Specification Clarifications

Number	SPECIFICATION CHANGES
	There are no Specification Clarifications in this revision of the specification update.

Documentation Changes

Number	SPECIFICATION CHANGES
	There are no Documentation Changes in this revision of the specification update.

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Errata

1. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHC with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

2. USB SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the "type" field for a SuperSpeed packet is set to a reserved value and the encoding for the "subtype" field is set to "ACK", the xHC may accept the packet as a valid acknowledgement transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

3. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None.

Status: No Plan to Fix

4. Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHC may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the TD (Transfer Descriptor)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is "0" or babble bytes

Implication: The xHC will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None.

Status: No Plan to Fix

5. xHCI Controller OC# Issue

Problem: xHCI Host Controller Reset (HCRST) may not complete if a USB over-current event occurs while powering on or resuming from S5 or S4.

Implication: Upon resume all xHCI Ports may become non-functional.

NOTE: To recover xHCI port funtionality requires the USB Device causing an overcurrent event to be removed and the system to be reset.

Workaround: None.

Status: No plan to fix.

6. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device dependent.

- Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

Workaround: None.

Status: No plan to fix.

7. USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event

Problem: After processing a USB 3.0 wake event, the USB xHCI controller may not re-enter D3 state.

Implication: When the failure occurs, the system will not enter an Sx state.

Workaround: Software should clear bit 28 PME Enable (PME_EN) of PMCRTL[28]PWR_CNTL_STS--Power management Control/Status Register (USB xHCI-D20:F0: Offset 74h) after the controller enters D0 state following an exit from D3.

For Microsoft* Windows 7, workaround is included in Intel® USB 3.0 eXtensible Host Controller Driver, version 4.0.0.23 or later.

For Microsoft* Windows 8.1, workaround is included in Intel® USB 3.0 Host Controller Adaptation Driver, version 1.0.0.27 or later.

Intel has notified all major OSV's of this behavior so this workaround may be implemented as needed.

Status: No plan to fix.

8. USB 3.0 Devices Not Detected After Sx Resume

Problem: While the system is in S3/S4/S5 and a USB 3.0 device is disconnected and reconnected to a system, the Cold Attach Status (CAS) bit 24 of PORTSCNUSB3-xHCI USB3 Port N Status and Control Register may be overwritten.

Implication: The system may not detect USB 3.0 devices after wake from S3/S4/S5.

Workaround: Software should issue a warm port reset when the PORTSCNUSB3-xHCI USB3 Port N Status and Control Register Port Link State (PLS) bits 8:5 is 0x7h(Link is in Polling State) and the CAS bit is 0.For Microsoft* Windows 7, workaround is included in Intel® USB 3.0 eXtensible Host Controller Driver, version 4.0.0.23 or later.

For Microsoft* Windows 8.1, workaround is included in Intel® USB 3.0 Host Controller Adaptation Driver, version 1.0.0.27 or later.

Intel has notified all major OSV's of this behavior so this workaround may be implemented as needed.

Status: No plan to fix.

9. PCI Express Unexpected Completion Status Bit May Get Set

Problem: A PCI Express Device replaying an Completion TLP may incorrectly cause an Unexpected Completion Error.

Note: This has only been observed when a PCIe device causes frequent link corruptions and recovery events to occur.

Implication: Bit 16 Unexpected Completion Status (UC) may get set in the UnCorrectable Error Status (UES) Register (PCI Express*-D28:F0/F1/F2/F3/F4/F5:offset 104h).

Workaround: System Software may set bit 16 Unexpected Completion Mask (UC) in the Uncorrectable Error Mask (UEM) Register (PCI Express*-D28:F0/F1/F2/F3/F4/F5:Offset 108h).

Status: No plan to fix.

10. eSPI Concurrent Get-Config and Flash Cycles

Problem: When an eSPI Get_Config cycle occurs concurrently with a flash cycle, the eSPI controller may stop working

Note: The issue has only been observed in a synthetic test environment only

Implication: System may hang

Workaround: None

Status: No Plan to Fix

11. xHCI U3 Wake exit Issue

Problem: xHCI Controller does not send the LFPS wake handshake for the full 10ms and reattempts U3 wakeup prior to the minimum 100ms wait time following a tNoLFPSResponseTimeout.

Note: USB3 Specification Section 7.5.9.2 Exit from U3 specifies the port shall remain in U3 when the 10-ms LFPS handshake timer times out (tNoLFPSResponseTimeout). And 7.2.4.2.7 Low Power Link State Exit Flow specifies a minimum of 100-ms delay between attempts to reinitiate U3 wakeup again.

Implication: Implication will be USB3 Super-Speed Device and OS / Host Driver dependent.

Note: Intel has Only observed this in a Synthetic Test Environment.

Workaround: None

Status: No Plan To Fix.

12. xHCI controller USB Debug Port Disconnect Issue

Problem: USB 3.0 Debug Port may hang when removing USB debug device.

Note: This issue has only been observed infrequently during USB debug connector unplug events

Implication: The Port will not function and require a Platform Reset to recover.

Workaround: None

Status: No Plan To Fix.

13. PSIC field incorrect value

Problem: PSIC (The Protocol Speed ID Count) field incorrectly reports a value of 3. PSIC should report 6 indicating SSIC support

Implication: If software utilizes PSIC, it may incorrectly determine SSIC is not supported. Additionally xHCI CV TD 1.09 Protocol Speed ID Test fails. Intel has obtained a waiver for PSIC.

Workaround: None Identified

Status: No Plan To Fix.

14. xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write

Problem: Bits [15:0] of xHCI Extended Capabilities CSR (Debug Capability Descriptor Parameters – XHCI_BAR, Offset 8740H) are incorrectly implemented as Read/Write, instead of Read-Only.

Implication: This erratum causes the USB-IF xHCI CV TD 1.05 Extended Capabilities Registers Tests to report a failure; Intel has obtained a waiver for TD1.05. Intel has not observed this erratum with any commercially available software.

Workaround: None

Status: No Plan To Fix.

15. SPI Dual I/O and Quad I/O Modes

Problem: When the PCH SPI controller is in Quad I/O or Dual I/O mode and reads a flash device which uses “mode cycles” after the address phase to enable the flash device’s special mode, the MISO, IO2, and IO3 signals will be pulled high by the PCH while the device expects the signals to be low

Implication: SPI transactions may fail resulting in possible system hang or failure during boot

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

16. eSPI Turn Around (TAR) Spec Violation

Problem: During the Turn Around (TAR) window, the eSPI controller does not drive the data lines to logic ‘1’ for the first clock as specified by the eSPI specification

Implication: There are no known functional failures due to this issue

Workaround: None

Status: No Plan to Fix

17. SMBus Transaction Using Memory Mapped I/O Registers

Problem: When using memory-mapped-I/O DATA register for a SMBus write transaction, data transmitted from the register for Byte Write, Block Write, or Send Byte operation with Packet Error Check (PEC) enabled may not match the data programmed by software.

Implication: The SMBus transaction may fail. Implication depends on the failing transaction.

Workaround: Platform software should use IO-mapped registers for SMBus transactions.

Status: No Plan to Fix

18. xHCI Host Controller USB 2.0 Control Transfer may cause IN Data to be dropped

Problem: USB 2.0 Control Transfers may incorrectly clear a USB 2.0 flow control condition to a USB 2.0 IN endpoint resulting in the dropping of IN Data to the flow controlled endpoint. Exposure is sensitive to high volume of unrelated OUT transactions occurring on the xHCI Host controller.

Implication: USB 2.0 Device dependent and may result in anomalous USB 2.0 Device behavior.

Note: Intel has only observed this with a single USB2.0 Device which frequently used USB 2.0 Control Transfers during operation

Workaround: None. A BIOS code change has been identified and may be implemented as a workaround to significantly minimize exposure to the occurrence of this erratum.

Status: No Plan To Fix.

19. System may hang while restoring HSIO ModPHY configuration

Problem: While Power Management Controller (PMC) is restoring High Speed I/O (HSIO) Modular Physical Layer (ModPHY) configuration during resume from S3, S4, S5 or while performing a platform reset the PMC may hang if a PMC managed timer expires during this time period.

Implication: System may hang during resume.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

20. xHCI Host Controller Reset May Cause a System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1 = ‘1’) the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Implication: CATERR may occur resulting in a system hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

21. PCI Express* Gen2 x4 Device may cause a Machine Check Exception

Problem: PCH PCI Express Host Controller when configured as Gen2 x4 may not properly handle an abrupt link transition to electrical idle without receiving Electrical Idle Ordered Set (EIOS) such as during hot unplug event.

Implication: Platform May Hang due to a Machine Check Exception if all of the following conditions are met when the link is terminated abruptly:

- No 8b10b errors occur,
- A TLP of exactly 3DWords is received (length started to count from STP as the first byte) **Note:** A valid TLP length is 5DWords at least),
- The TLP must end with END or EDB,
- And dependent on the specific internal timing of the DW alignment.

Workaround: None

Status: No Plan To Fix.

22. PCH PCIe* Controller Root Port Access Control Services Control Registers (ACSCTLR) Appear as Read Only

Problem: ACSCTLR is implemented and documented in the External Design Specification (EDS) at Offset 0x148 instead of at Offset 0x146 as documented in the PCI-SIG PCI Express® Base Specification

Implication: ACS aware software will not be able to access and configure ACSCTLR at Offset 0x146

Workaround: ACS aware software must account for and access ACSCTLR at Offset 0x148 as documented in the Datasheet.

Status: No Plan To Fix.

23. Pull-up and Pull-down on SPI CS# and CLK Signals

Problem: The pull up/pull down implementation before RSMRST# assertion on SPI chip select (CS#) and clock (CLK) signals does not match the specified behavior. The actual implementation has no pull-up or pull down before RSMRST# assertion.

Implication: System implication depends on the external device requirements sampling the SPI CS# and CLK signals.

Workaround: Implement an external pull-up, depending on the external device requirements.

Status: No Plan to Fix.
The correct implementation information will be updated in Revision 002 of the 6th Generation Intel Processor Families IO Platform Datasheet.

24. eSPI Error Reporting

Problem: When errors occur on the eSPI interface, the eSPI error reporting registers (VWERR_SLV, LNKERR_SLV, FCERR_SLV, PCERR_SLV, SLV_CFG_REG_CTL) may not be updated correctly.

Implication: Platform implication depends on the software usage of the registers.

Workaround: None

Note: eSPI error handling software may issue an in-band reset to the eSPI device when detecting an error associated with these registers.

Status: No Plan to Fix.

25. USB 3.0 DCI Control Packet issue

Problem: DbC (Debug Capability) Device connection may hang if the USB 3.0 host controller DCI (Direct Connect Interface) does not send Control Packets in multiples of 16.

Implication: USB 3.0 host controller DCI may hang.

Workaround: DbC software must ensure DCI Control Packets are sent in multiples of 16. And no concurrent OUT EP traffic is occurring while the Control Packets are in progress to the DCI device.

Status: No Plan to fix

26. eSPI Fatal Error Handling

Problem: The eSPI controller may not correctly handle fatal errors occurring on the eSPI bus.

Implication: System implication depends on the type of the fatal error and may result in a system hang.

Note: A fatal error is a rare event on the eSPI interface and this issue has only been observed by Intel in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix

27. PCH PCIe* TX Pin State During L1.0 and L1.1 Substates

Problem: Upon entry to L1.0 or L1.1 Substates the PCH PCIe* TX pins may internally get pulled down to ground instead of maintaining the link common mode voltage

Implication: PCIe* devices that are in L1.0 or L1.1 may interpret the grounding of the TX pins as an exit event from electrical idle which may cause them to assert their CLKREQ# and exit the L1 Power Management

Notes:

- The issue has only been observed with a single 3rd Party PCIe* Device
- The issue is depended on the end point device input squelch sensitivity and if the device sends a Latency Tolerance and Reporting (LTR) Snoop/Non-Snoop Latency Message above 50 Microseconds while entering L1.0 or L1.1 with CLKREQ# de-asserted

Workaround: None

Status: No Plan to Fix

28. Subsequent Deep S5 and S5 Exits Impacted After "Straight to S5 (Host Stays There)" Resets

Problem: Following a S0 resume from a "Straight to S5 (Host Stays There)" reset, the PCH may enforce earlier wake event restrictions from the "Straight to S5 (Host Stays There)" reset on subsequent Deep S5 and S5 exits causing some wake events not to be recognized by the PCH.

Note: This issue only occurs on platforms where Deep S5 is enabled. This issue does not impact S3/S4 exits.

Implication:

- On subsequent Deep S5 exits, the following events will not be able to wake the system:
  - — RTC Alarm, PCIe WAKE# pin, and Wake Alarm Device.
- On subsequent S5 exits if the S5 entry is due leaving Deep Sx because of ACPRESENT assertion, the following events will not be able to wake the system:
  - — RTC Alarm, PCIe WAKE# pin, Wake Alarm Device, GPIOs and Secondary PME#
- If system is in S5 for any other reason, this issue will not be present.

Workaround: None

Note: The Deep S5 / S5 exit restrictions will be cleared after DSW_PWROK assertion (G3 power state) or after another global reset occurs (as long as global reset is not of the type "Straight to S5 (Host Stays There)").

Status: No Plan to Fix

29. eSPI Bus Mastering

Problem: The eSPI controller may not successfully complete bus mastering cycles from a slave device as described below:

1. Upstream memory write from EC may have the last DW dropped if there's an upstream completion of a configuration cycle occurring at the same time
2. The controller may prevent the system from entering a warm reset if an upstream non-posted cycle is pending
3. The controller may not perform ordering between posted/non-posted/completion requests

The issue has only been observed in synthetic testing environment

Implication: System may hang

Workaround: None

Status: No Plan to Fix.

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Specification Changes

There are no Specification Changes in this revision of the specification update.

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Specification Clarifications

There are no Specification Changes in this revision of the Specification Update.

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Documentations Changes

There are no Documentation Changes in this revision of the Specification Update.

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