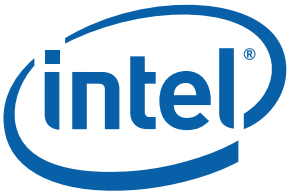

Intel® Xeon® Processor E7-4800/8800 v3 Product Families

Boundary Scan Descriptor Language (BSDL) Readme

May 2015

Reference Number.: 332319-001US

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Revision History

Document Number	Revision Number	Description	Date
332319	001	• Initial Release	May 2015

Overview

Scope

This document is intended for the development of IEEE 1149 Boundary Scan Tests for the Intel® Xeon® Processor E7-4800/8800 v3 Product Families. This Readme assumes a working knowledge of IEEE 1149 methodologies and the In Circuit Test (ICT) manufacturing test methods.

This release package supports the processor steppings shown in the table below.

Table 1. BSDL File Summary

• HSW_EX_E0.bsdl	Full Boundary Scan File

Related Documents

Refer to the following documents for additional processor information.

Table 2. Related Documents

Document	Document Number/Location
IEEE Standard Test Access Port and Boundary Scan Architecture Specification	http://standards.ieee.org

Readme

Full Boundary-Scan

After applying voltage to the power pins, the following initialization sequence must be completed prior to TAP accesses during application of the boundary-scan test patterns:

a. BCLK[1:0]_D[P/N] continuous toggle at 100 MHz

b. VMSE_PWR_OK, PWRGOOD, RESET_N are initialized LOW.

c. All power supplies are up.

d. VMSE_PWR_OK is driven HIGH and remains driven HIGH for the duration of the boundary-scan test pattern execution

e. EAR_N pin is initialized HIGH.

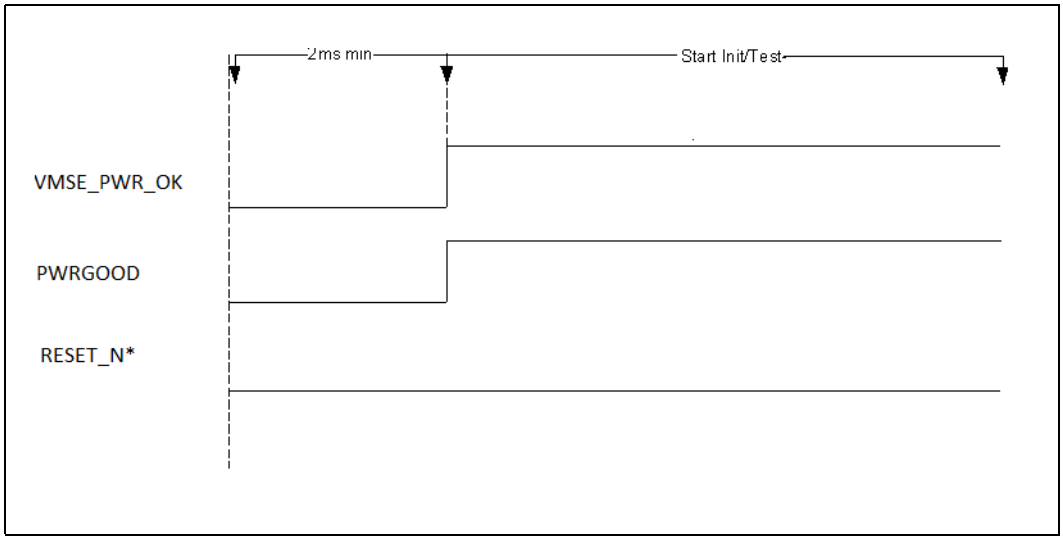
f. PROCHOT_N pin is initialized HIGH.

g. EAR_N and PROCHOT_N need to be initialized HIGH (de-asserted) prior to PWRGOOD assertion

h. PWRGOOD pin must be driven HIGH 2 ms after power pins are stable and remain drive HIGH for the duration of the boundary-scan test pattern execution.

i. RESET_N pin should be driven LOW for the duration of the boundary-scan test pattern execution.

Figure 1. Reset Sequence



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